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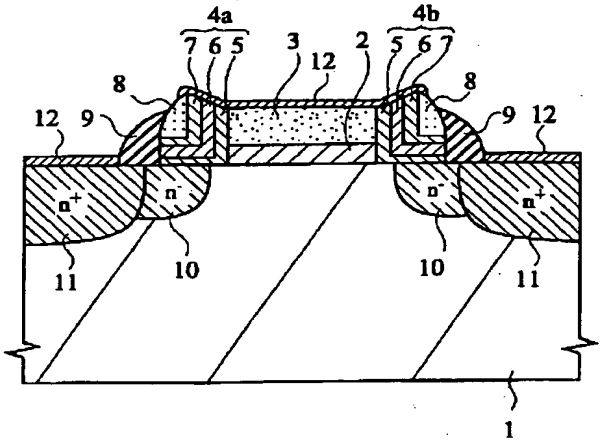
(54)【発明の名称】　半導体記憶装置およびその製造方法

(57)【要約】
【課題】　簡単なセル構造で複数ビット分の情報を記憶することができる不揮発性半導体記憶装置を提供する。
【解決手段】　複数ビット分の情報を記憶することができる不揮発性半導体記憶装置の新規な構造であり、ゲート電極の端部に電子を蓄積する電荷蓄積層４を有している。電荷蓄積層４に電子を蓄積することで、複数ビット分の情報を記憶する。



1

【特許請求の範囲】

【請求項１】　半導体基板の主面上に、ゲート絶縁膜を介して、配置された第１のゲート電極と、

該第１のゲート電極の側面上に配置された電荷蓄積層と、

前記第１のゲート電極の側面上に、前記電荷蓄積層を介して、配置された第２のゲート電極と、

前記第１のゲート電極と前記第２のゲート電極とを、電気的に接続する導電層とを有することを特徴とする不揮発性半導体記憶装置。

【請求項２】　半導体基板の主面上に、ゲート絶縁膜を介して、第１のゲート電極を形成する工程と、

前記第１のゲート電極の側面上に電荷蓄積層および第２のゲート電極を、順次形成する工程と、

前記第１のゲート電極と前記第２のゲート電極とを、電気的に接続する導電層を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。

【請求項３】　半導体基板の主面上に配置された、第１、第２および第３の絶縁膜から成る、ゲート絶縁膜と、

前記第２の絶縁膜の端部に配置された電荷蓄積層と、

前記ゲート絶縁膜上に配置されたゲート電極とを有することを特徴とする不揮発性半導体記憶装置。

【請求項４】　半導体基板の主面上に、第１、第２および第３の絶縁膜を順次形成し、該第１、第２および第３の絶縁膜から成るゲート絶縁膜を形成する工程と、

該ゲート絶縁膜の上部にゲート電極構成材料を堆積した後、該ゲート電極構成材料およびゲート絶縁膜をパターニングすることで、ゲート電極を形成する工程と、

前記第２の絶縁膜の端部を選択的に除去し、空間を形成する工程と、

該空間に電荷蓄積層を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法

【請求項５】　半導体基板の主面上に配置された第１の下部絶縁膜、該第１の下部絶縁膜の中央の上部に配置された第１の中間絶縁膜、前記第１の下部絶縁膜の端部の上部に配置された第１の電荷蓄積層、前記第１の中間絶縁膜および第１の電荷蓄積層の上部に配置された第１の上部絶縁膜、および、該第１の上部絶縁膜の上部に配置された第１のゲート電極、とを有する不揮発性半導体記憶装置と、

前記半導体基板の主面上に配置された、前記第１の中間絶縁膜と同一材料から成る第２の下部絶縁膜、前記半導体基板の主面上に、かつ該第２の下部絶縁膜の両端に配置された極薄絶縁膜、該極薄絶縁膜の上部に配置された、前記第１の電荷蓄積層と同一材料から成る第２の電荷蓄積層、前記第２の下部絶縁膜および第２の電荷蓄積層の上部に配置された、前記第１の上部絶縁膜と同一材料から成る第２の上部絶縁膜、および、該第２の上部絶

2

縁膜の上部に配置された第２のゲート電極、とを有する揮発性半導体記憶装置とを具備することを特徴とする半導体記憶装置。

【請求項６】　半導体基板の主面上に配置された第１の下部絶縁膜、該第１の下部絶縁膜の中央の上部に配置された第１の中間絶縁膜、前記第１の下部絶縁膜の端部の上部に配置された第１の電荷蓄積層、前記第１の中間絶縁膜および第１の電荷蓄積層の上部に配置された第１の上部絶縁膜、該第１の上部絶縁膜の上部に配置された第１のゲート電極、とを有する不揮発性半導体記憶装置と、

前記半導体基板の主面上に配置された極薄絶縁膜、該極薄絶縁膜上に配置された、前記第１の電荷蓄積層と同一材料から成る第２の電荷蓄積層、該第２の電荷蓄積層上に配置された第２の上部絶縁膜、該第２の上部絶縁膜上に配置された第２のゲート電極、とを有する揮発性半導体記憶装置とを具備することを特徴とする半導体記憶装置。

【請求項７】　半導体基板の主面上に配置された下部絶縁膜と、

前記半導体基板の主面上に、かつ該下部絶縁膜の両端に配置された極薄絶縁膜と、

該極薄絶縁膜の上部に配置された電荷蓄積層と、

前記下部絶縁膜および電荷蓄積層の上部に配置された上部絶縁膜と、

該上部絶縁膜の上部に配置されたゲート電極とを有することを特徴とする揮発性半導体記憶装置。

【請求項８】　半導体基板の主面上に配置された極薄絶縁膜と、

該極薄絶縁膜上に配置された電荷蓄積層と、

該電荷蓄積層上に配置された絶縁膜と、

該絶縁膜上に配置されたゲート電極とを有することを特徴とする揮発性半導体記憶装置。

【請求項９】　半導体基板の主面上の一部に、第１の絶縁膜を形成する工程と、

該第１の絶縁膜の上部および前記半導体基板の主面の一部以外に、第２および第３の絶縁膜を順次形成する工程と、

該第３の絶縁膜の上部にゲート電極構成材料を堆積する工程と、

該ゲート電極構成材料、前記第３の絶縁膜、前記第２の絶縁膜および第１の絶縁膜をパターニングすることで、第１のゲート電極を形成する工程と、

前記ゲート電極構成材料、前記第３の絶縁膜および第２の絶縁膜をパターニングすることで、第２のゲート電極を形成する工程と、

該第１および第２のゲート電極の両方の第２の絶縁膜の端部を選択的に除去し、空間を形成する工程と、

該空間に電荷蓄積層を形成する工程とを少なくとも含むことを特徴とする半導体記憶装置の製造方法。

【請求項１０】　半導体基板の主面上に、第１、第２および第３の絶縁膜を順次形成する工程と、
該第３の絶縁膜の上部に第１のゲート電極構成材料を堆積した後、該ゲート電極構成材料、前記第３の絶縁膜、前記第２の絶縁膜および第１の絶縁膜をパターニングすることで、第１のゲート電極を形成する工程と、
該第１のゲート電極形成工程と同時に行われる工程であって、前記半導体基板の主面の一部に、前記ゲート電極構成材料、前記第３の絶縁膜、前記第２の絶縁膜および第１の絶縁膜を除去することで、第２のゲート電極形成領域を形成する工程と、
前記第１のゲート電極の第２の絶縁膜の端部を選択的に除去し、空間を形成する工程と、
前記半導体基板の主面上に、極薄絶縁膜を形成する工程と、
前記半導体基板の主面上に、電荷蓄積層を構成する材料を堆積した後、該電荷蓄積層構成材料を異方性エッチングすることで、前記第１のゲート電極の空間に電荷蓄積層を形成する工程と、
前記半導体基板の主面上に、第４の絶縁膜および第２のゲート電極構成材料を堆積した後、該第２のゲート電極構成材料、前記第４の絶縁膜、前記電荷蓄積層構成材料および極薄絶縁膜をパターニングすることで、第２のゲート電極を形成する工程とを少なくとも含むことを特徴とする半導体記憶装置の製造方法。
【請求項１１】　半導体基板の主面上に配置された凸部と、
該凸部を含む前記半導体基板の主面上に配置された、第１、第２および第３の絶縁膜から成る、ゲート絶縁膜と、
前記第２の絶縁膜の端部に配置された電荷蓄積層と、
前記ゲート絶縁膜上に配置されたゲート電極とを有することを特徴とする不揮発性半導体記憶装置。
【請求項１２】　半導体基板の主面上に、凸部を形成する工程と、
該凸部を含む前記半導体基板の主面上に、第１、第２および第３の絶縁膜を順次形成し、該第１、第２および第３の絶縁膜から成るゲート絶縁膜を形成する工程と、
該ゲート絶縁膜の上部にゲート電極構成材料を堆積した後、該ゲート電極構成材料およびゲート絶縁膜をパターニングすることで、ゲート電極を形成する工程と、
前記第２の絶縁膜の端部を選択的に除去し、空間を形成する工程と、
該空間に電荷蓄積層を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。
【請求項１３】　半導体基板の主面上に配置された凸部と、
該凸部を含む前記半導体基板の主面上に配置された、第１および第２の絶縁膜から成る、ゲート絶縁膜と、
該第１および第２の絶縁膜の間に配置された電荷蓄積層と、
前記ゲート絶縁膜上に配置されたゲート電極とを有することを特徴とする不揮発性半導体記憶装置。

【請求項１４】　半導体基板の主面上に、凸部を形成する工程と、
該凸部を含む前記半導体基板の主面上に、第１の絶縁膜、電荷蓄積層構成材料、および第３の絶縁膜を順次形成する工程と、
該第１の絶縁膜、電荷蓄積層構成材料および第３の絶縁膜をパターニングすることで、ゲート電極を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。
【請求項１５】　半導体基板の主面上に配置された凹部と、
該凹部を含む前記半導体基板の主面上に配置された、第１、第２および第３の絶縁膜から成る、ゲート絶縁膜と、
前記第２の絶縁膜の端部に配置された電荷蓄積層と、
前記ゲート絶縁膜上に配置されたゲート電極とを有することを特徴とする不揮発性半導体記憶装置。
【請求項１６】　半導体基板の主面上に、凹部を形成する工程と、
該凹部を含む前記半導体基板の主面上に、第１、第２および第３の絶縁膜を順次形成し、該第１、第２および第３の絶縁膜から成るゲート絶縁膜を形成する工程と、
該ゲート絶縁膜の上部にゲート電極構成材料を堆積した後、該ゲート電極構成材料およびゲート絶縁膜をパターニングすることで、ゲート電極を形成する工程と、
前記第２の絶縁膜の端部を選択的に除去し、空間を形成する工程と、
該空間に電荷蓄積層を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。
【請求項１７】　半導体基板の主面上に配置された凹部と、
該凹部を含む前記半導体基板の主面上に配置された、第１および第２の絶縁膜から成る、ゲート絶縁膜と、
該第１および第２の絶縁膜の間に配置された電荷蓄積層と、
前記ゲート絶縁膜上に配置されたゲート電極とを有することを特徴とする不揮発性半導体記憶装置。
【請求項１８】　半導体基板の主面上に、凹部を形成する工程と、
該凸部を含む前記半導体基板の主面上に、第１の絶縁膜、電荷蓄積層構成材料、および第３の絶縁膜を順次形成する工程と、
該第１の絶縁膜、電荷蓄積層構成材料および第３の絶縁膜をパターニングすることで、ゲート電極を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。
【請求項１９】　半導体基板の主面上に、凹部を形成す

る工程と、
該凹部を含む前記半導体基板の主面上に、第１、第２および第３の絶縁膜を順次形成し、該第１、第２および第３の絶縁膜から成るゲート絶縁膜を形成する工程と、
該ゲート絶縁膜の上部にゲート電極構成材料を堆積した後、該ゲート電極構成材料を化学的機械的研磨方法で除去することで、前記凹部に埋め込まれたゲート電極を形成する工程と、
前記第２の絶縁膜の端部を選択的に除去し、空間を形成する工程と、
該空間に電荷蓄積層を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。
【請求項２０】　半導体基板の主面上に、凹部を形成する工程と、
該凹部を含む前記半導体基板の主面上に、第１の絶縁膜、電荷蓄積層構成材料、および第３の絶縁膜を順次形成する工程と、
該第３の絶縁膜の上部にゲート電極構成材料を堆積した後、該ゲート電極構成材料を化学的機械的研磨方法で除去することで、前記凹部に埋め込まれたゲート電極を形成する工程とを少なくとも含むことを特徴とする不揮発性半導体記憶装置の製造方法。
【請求項２１】　半導体基板の主面上に、ゲート絶縁膜を介して、配置されたゲート電極と、
該ゲート電極の端部に配置された凹部と、
該凹部に、絶縁膜を介して、かつ、チャネル領域およびソースドレイン領域の両方の上部に配置された電荷蓄積層とを有することを特徴とする不揮発性半導体記憶装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、電気的に書き込み消去可能な不揮発性半導体記憶装置およびその製造方法、高速に書き込み読み出し可能な揮発性半導体記憶装置およびその製造方法、ならびに不揮発性半導体記憶装置と揮発性半導体記憶装置を同一チップ上に混載した半導体記憶装置およびその製造方法に関する。
【０００２】
【従来の技術】従来のＥＥＰＲＯＭ（Electrically Erasable and Programmable Read Only Memory）等の不揮発性メモリでは、１つのセルに異なる２つのしきい値を実現することで、１つのセルに１ビット分の情報を記憶する。これに対してメモリ高密度化のため、１つのセルに４つ以上のしきい値を持たせ、２ビット分以上の情報を１つのセルに記憶する技術が提案されている（M. Bauer et al., ISSCC95, p.132）。しかし、この技術を実現するには、しきい値電圧の正確な制御、しきい値電圧の小さな変化分の正確な検知、さらに従来以上の電荷保持信頼性が要求される。したがって、この技術では、実際には必ずしも従来と同等の性能を得ることはできない。また、この技術は、製造歩留りが低いという問題もある。このため、電荷を物理的に異なる複数の位置に蓄積することで複数ビット分の情報を記憶するセル構造が新たに提案されている（B. Eitan et al, IEDM96, p169, Fig6）。また、それに類似のセル構造として本発明者によってゲート電極の側壁に電荷蓄積層を設ける構造が以前に提案されている（米国特許番号第４８８１１０８号）。しかし、それらセル構造の製造工程は非常に複雑なものであり、またチャネル領域の制御性も十分ではないという問題がある。
【０００３】一方、昨今のシステム・オン・チップの要求から電気的に書き込み消去可能な不揮発性メモリと高速に書き込み読み出し可能な揮発性メモリを同一のチップ上に実現する必要が高まっている。特に、ＥＥＰＲＯＭやフラッシュメモリ等の浮遊ゲート構造を有する不揮発性メモリと高速動作可能なダイナミックＲＡＭを混載するＶＬＳＩの要求が急増している。ところが、近年のダイナミックＲＡＭのメモリセルはトレンチ構造やスタック構造といった非常に複雑な３次元構造となってきている。このため、浮遊ゲート型不揮発性メモリとダイナミックＲＡＭを混載しようとすれば、そのメモリセル構造の違いから、製造プロセスは複雑化し、マスク工程数も増大する。したがって、その混載チップの製造コストは非常に大きなものとなってしまう。
【０００４】浮遊ゲート型の不揮発メモリのメモリセル構造を用いてダイナミックＲＡＭのメモリセルを実現すれば、セル構造の共通化によって、製造プロセスは単純化され、製造コストを低減することは可能である。しかし、その共通化されたメモリセルではダイナミックＲＡＭの特徴である高速書き込みを実現することは困難である。
【０００５】
【発明が解決しようとする課題】本発明は、上記事情に鑑みて成されたものであり、簡単なセル構造で複数ビット分の情報を記憶することができる不揮発性半導体記憶装置の構造を提供することを目的とする。
【０００６】本発明の他の目的は、簡単な製造プロセスで複数ビット分の情報を記憶する不揮発性半導体記憶装置を製造する不揮発性半導体記憶装置の製造方法を提供することである。
【０００７】本発明のさらに他の目的は、簡単なセル構造で電気的に書き込み消去可能な不揮発性メモリと高速書き込み読み出し可能な揮発性メモリを混載した半導体記憶装置の構造を提供することである。
【０００８】本発明のさらに他の目的は、簡単な製造プロセスで電気的に書き込み消去可能な不揮発性メモリと高速書き込み読み出し可能な揮発性メモリを混載した半導体記憶装置の製造方法を提供することである。
【０００９】
【課題を解決するための手段】上記目的を達成するため

に、本発明の第１の特徴は、半導体基板の主面上に、ゲート絶縁膜を介して、配置された第１のゲート電極と、第１のゲート電極の側面上に配置された電荷蓄積層と、第１のゲート電極の側面上に、電荷蓄積層を介して、配置された第２のゲート電極と、第１のゲート電極と第２のゲート電極とを、電気的に接続する導電層と、を少なくとも具備する不揮発性半導体記憶装置であることである。

【００１０】本発明の第２の特徴は、半導体基板の主面上に配置された、第１、第２および第３の絶縁膜から成る、ゲート絶縁膜と、第２の絶縁膜の端部に配置された電荷蓄積層と、ゲート絶縁膜上に配置されたゲート電極と、を少なくとも具備する不揮発性半導体記憶装置であることである。

【００１１】本発明の第３の特徴は、不揮発性半導体記憶装置と揮発性半導体記憶装置とを混載する半導体記憶装置であって、不揮発性半導体記憶装置は、半導体基板の主面上に配置された第１の下部絶縁膜と、第１の下部絶縁膜の中央の上部に配置された第１の中間絶縁膜と、第１の下部絶縁膜の端部の上部に配置された第１の電荷蓄積層と、第１の中間絶縁膜および第１の電荷蓄積層の上部に配置された第１の上部絶縁膜と、第１の上部絶縁膜の上部に配置された第１のゲート電極と、を少なくとも具備し、揮発性半導体記憶装置は、半導体基板の主面上に配置された、第１の中間絶縁膜と同一材料から成る第２の下部絶縁膜と、半導体基板の主面上に、かつ第２の下部絶縁膜の両端に配置された極薄絶縁膜と、極薄絶縁膜の上部に配置された、第１の電荷蓄積層と同一材料から成る第２の電荷蓄積層と、第２の下部絶縁膜および第２の電荷蓄積層の上部に配置された、第１の上部絶縁膜と同一材料から成る第２の上部絶縁膜と、第２の上部絶縁膜の上部に配置された第２のゲート電極と、を少なくとも具備する。

【００１２】本発明の第４の特徴は、不揮発性半導体記憶装置と揮発性半導体記憶装置とを混載する半導体記憶装置であって、不揮発性半導体記憶装置は、半導体基板の主面上に配置された第１の下部絶縁膜と、第１の下部絶縁膜の中央の上部に配置された第１の中間絶縁膜と、第１の下部絶縁膜の端部の上部に配置された第１の電荷蓄積層と、第１の中間絶縁膜および第１の電荷蓄積層の上部に配置された第１の上部絶縁膜と、第１の上部絶縁膜の上部に配置された第１のゲート電極と、を少なくとも具備し、揮発性半導体記憶装置は、半導体基板の主面上に配置された極薄絶縁膜と、極薄絶縁膜上に配置された、第１の電荷蓄積層と同一材料から成る第２の電荷蓄積層と、第２の電荷蓄積層上に配置された第２の上部絶縁膜と、第２の上部絶縁膜上に配置された第２のゲート電極と、を少なくとも具備する。

【００１３】本発明の第５の特徴は、半導体基板の主面上に配置された凸部または凹部と、凸部または凹部を含む半導体基板の主面上に配置された、第１、第２および第３の絶縁膜から成る、ゲート絶縁膜と、第２の絶縁膜の端部に配置された電荷蓄積層と、ゲート絶縁膜上に配置されたゲート電極と、を少なくとも具備する不揮発性半導体記憶装置であることである。

【００１４】本発明の第６の特徴は、半導体基板の主面上に配置された凸部または凹部と、凸部または凹部を含む半導体基板の主面上に配置された、第１および第２の絶縁膜から成る、ゲート絶縁膜と、第１および第２の絶縁膜の間に配置された電荷蓄積層と、ゲート絶縁膜上に配置されたゲート電極と、を少なくとも具備する不揮発性半導体記憶装置であることである。

【００１５】本発明の第７の特徴は、半導体基板の主面上に、ゲート絶縁膜を介して、配置されたゲート電極と、ゲート電極の端部に配置された凹部と、凹部に、絶縁膜を介して、配置された電荷蓄積層を、を少なくとも具備し、電荷蓄積層は、チャネル領域およびソースドレイン領域の両方の上部に配置される不揮発性半導体記憶装置であることである。

【００１６】

【発明の実施の形態】以下図面を参照して、本発明の実施の形態を説明する。以下の図面の記載において、同一または類似の部分には同一または類似の符号を付している。ただし、図面は模式的なものであり、厚みと平面寸法との関係、各層の厚みの比率等は現実のものとは異なることに留意すべきである。したがって、具体的な厚みや寸法は以下の説明を参酌して判断すべきものである。また図面相互間においても互いの寸法の関係や比率が異なる部分が含まれていることはもちろんである。

【００１７】（第１の実施の形態）図１は、本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。このメモリセルは、ｎ型ＭＯＳトランジスタで構成される。本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセル構造では、ｐ型半導体基板１の表面にゲート絶縁膜２を介して第１ゲート電極３が設けられ、第１ゲート電極３の両側面には電荷蓄積層４（４ａ，４ｂ）が設けられる。この電荷蓄積層４は積層構造を有しており、第１層が第１酸化膜５、第２層が窒化膜６、第３層が第２酸化膜７で構成される。さらに、電荷蓄積層４の上部には第２ゲート電極８が設けられる。電荷蓄積層４の側面にはサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１には、チャネル領域に接する低不純物濃度のｎ$^{-}$型拡散層１０と、このｎ$^{-}$型拡散層１０の外側に位置する高不純物濃度のｎ$^{+}$型拡散層１１が設けられる。第１ゲート電極３、電荷蓄積層４、第２ゲート電極８およびｎ$^{+}$型拡散層１１それぞれの表面には導電層１２が設けられる。第１ゲート電極３と第２ゲート電極８はこの導電層１２を介して電気的に接続される。

【００１８】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ⁻型拡散層１０と高不純物濃度のｎ⁺型拡散層１１で構成したＬＤＤ（Lightly doped drain）構造を有している。そして、第１ゲート電極３の両側面には電荷蓄積層４が形成され、この２つの電荷蓄積層４の窒化膜６に保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。さらに、電荷蓄積層４の上部に第２ゲート電極８を形成し、この第２のゲート電極８を第１ゲート電極３に電気的接続することで、チャネル領域の制御性を高め、しきい値電圧変化分の検知を容易にする。

【００１９】次に、本発明の第１の実施の形態に係る不揮発性メモリの動作について図２乃至図４を用いて説明する。図２は、書き込み動作を説明する不揮発性メモリの断面図である。図３は、読み出し動作を説明する不揮発性メモリの断面図である。図４は、消去動作を説明する不揮発性メモリの断面図である。図２に示すように、メモリセルの書き込み時には、ゲートＧに高電圧（～１０Ｖ）を印加し、同時に電子を蓄積する電荷蓄積層４ｂに近接するドレインＤに高電圧（～８Ｖ）を加え、近接しないソースＳを接地する。このように電圧を印加すると、チャネル熱電子（Channel Hot Electron）が発生し、この熱電子が電荷蓄積層４ｂの窒化膜６に捕獲される。電荷蓄積層４ｂに電子が捕獲されると、セルトランジスタのしきい値電圧が変化する。メモリセルの読み出しは、しきい値電圧の変化分を検知することで行われる。具体的には、図３に示すように、ゲートＧに電圧５Ｖを加え、同時にドレインＤに電圧３Ｖを印加し、電流量の差をセンスアンプによって検知する。また、メモリセルの消去は、図４に示すように、ゲートＧに負電圧（～－６Ｖ）を印加し、消去される電荷蓄積層４ｂに近接するドレインＤに正電圧（～９Ｖ）を印加し、電荷蓄積層４ｂに捕獲された電子を放出することで行われる。なお、周知の通り、ＭＯＳトランジスタのソースＳとドレインＤとは対称に出来ており、一般にソースＳとドレインＤとは入れ換えることが可能である。したがって、上記の説明においても、ソースＳとドレインＤを入れ換えることが可能である。

【００２０】次に、本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造方法を図５乃至図９を用いて説明する。まず図５に示すように、ｐ型半導体基板１上に熱酸化によって２５ｎｍのゲート絶縁膜２を形成する。続いて、ｐ型半導体基板１全面にＬＰＣＶＤ（Low Pressure Chemical Vapor Deposition）法によりｎ型またはｐ型不純物をドープした３００ｎｍの多結晶シリコン膜を堆積した後、周知の露光技術およびエッチング技術によりパターニングし、第１ゲート電極３を形成する。

【００２１】次に、図６に示すように、ソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面のゲート絶縁膜２を除去した後、ｐ型半導体基板１を９００℃～１２００℃の酸化雰囲気中で熱酸化し、１０ｎｍの第１酸化膜５を形成する。そして、第１酸化膜５上にＬＰＣＶＤ法により１０ｎｍ～１００ｎｍの窒化膜６を堆積し、その後９００℃の水素燃焼酸化あるいはＣＶＤ法により窒化膜６表面に５ｎｍ程度の第２酸化膜７を形成する。

【００２２】次に、図７に示すように、第２酸化膜７上にたとえばＬＰＣＶＤ法により２５～２５０ｎｍ程度の多結晶シリコンを堆積した後、ＲＩＥ（Reactive Ion Etching）法による異方性エッチングを行い、この多結晶シリコン膜、第１酸化膜５、窒化膜６および第２酸化膜７をそれらの膜厚分だけ除去することで、上部に第２ゲート電極８を有する電荷蓄積層４を第１ゲート電極側面に形成する。

【００２３】次に、図８に示すように、低不純物濃度のｎ⁻型拡散層１０を形成する。ｎ⁻型拡散層１０はイオン注入技術により第１ゲート電極３および電荷蓄積層４をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成される。

【００２４】次に、図９に示すように、電荷蓄積層４の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｎ⁺型拡散層１１を形成する。ｎ⁺型拡散層１１はイオン注入技術により第１ゲート電極３、電荷蓄積層４およびサイドウォールスペーサ９をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成される。

【００２５】次に、ｐ型半導体基板１の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｐ型半導体基板１を不活性雰囲気中で熱処理することにより第１ゲート電極３、電荷蓄積層４、第２ゲート電極８およびｎ⁺型拡散層１１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。この時、第１ゲート電極３および第２ゲート電極８上の高融点金属シリサイド層がブリッジングするように、第１酸化膜５、窒化膜６、第２酸化膜７、特に、窒化膜６の膜厚が設定されている必要がある。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図１に示したメモリセル構造が完成する。

【００２６】なお、図示はしないが、図１のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【００２７】本発明の第１の実施の形態によれば、電荷蓄積層４の上部にも第２ゲート電極８を設けたので、しきい値電圧の制御性が向上する。なお、本発明の第１の

実施の形態では、メモリセルをｎ型ＭＯＳトランジスタで構成する場合について説明したが、ｐ型ＭＯＳトランジスタで構成する場合であっても同様の効果が得られる。また、メモリセルはＬＤＤ構造を有しているが、シングルドレイン構造、ダブルドレイン構造であっても構わない。

【００２８】（第２の実施の形態）次に、本発明の第２の実施の形態を説明する。図１０は、本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。このメモリセルはｎ型ＭＯＳトランジスタで構成される。本発明の第２の実施の形態に係る不揮発性メモリのメモリセル構造では、ｐ型半導体基板１の表面に第１ゲート絶縁膜１３を介して第２ゲート絶縁膜１４が設けられる。そして、第２ゲート絶縁膜１４の両端には電荷蓄積層４ａ、４ｂが形成される。第２ゲート絶縁膜１４および電荷蓄積層４ａ、４ｂ上には第３ゲート絶縁膜１５を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１には、チャネル領域に接する低不純物濃度のｎ$^-$型拡散層１０と、このｎ$^-$型拡散層１０の外側に位置する高不純物濃度のｎ$^+$型拡散層１１が設けられる。ゲート電極３およびｎ$^+$型拡散層１１それぞれの表面には導電層１２が設けられる。

【００２９】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ$^-$型拡散層１０と高不純物濃度のｎ$^+$型拡散層１１で構成したＬＤＤ構造を有している。そして、ゲート絶縁膜が第１ゲート絶縁膜１３（下層）、第２ゲート絶縁膜１４（中間層）および第３ゲート絶縁膜１５（上層）からなる３層積層膜で構成され、第２ゲート絶縁膜１４の両端部には電荷蓄積層４ａおよび４ｂが形成される。この２つの電荷蓄積層４ａおよび４ｂに電子を蓄積し、その蓄積状態は（１）電荷蓄積層４ａ、４ｂのいずれも電子を蓄積していない状態、（２）電荷蓄積層４ａのみが電子を蓄積している状態、（３）電荷蓄積層４ｂのみが電子を蓄積している状態、（４）電荷蓄積層４ａ、４ｂ共に電子を蓄積している状態、の４つの状態をとり得る。この２つの電荷蓄積層４ａおよび４ｂに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。また、このメモリセル構造では電荷蓄積層４ａ、４ｂはチャネル領域端部の上方に位置するので、チャネル領域中央部のしきい値電圧はチャネル領域の不純物濃度のみで決まり、電荷蓄積層４ａ、４ｂの電子の蓄積状態に依存しない。したがって、電荷蓄積層４ａ、４ｂの電子の過不足による過消去（over-erase）は防止され、それにより過消去に起因するリーク不良、プログラム不良、読み出し不良等は生じ得ない。また、ソース領域とドレイン領域間のリーク電流はゲート電圧のみで抑制でき、高信頼性の不揮発性半導体メモリを実現できる。電荷蓄積層４ａおよび４ｂはＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第１ゲート絶縁膜１３、第３ゲート絶縁膜１５をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度なので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細化のみならず周辺高電圧動作素子の微細化も可能となる。

【００３０】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｎ$^-$型拡散層１０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を構成してもよい。第２ゲート絶縁膜１４は電荷蓄積層４ａ－４ｂ間のリークを防止するが、たとえばシリコン酸化膜で構成することができる。また、第２ゲート絶縁膜１４に高誘電率を有する金属酸化膜を用いれば、チャネル領域中央の電流伝達特性を向上できる。金属酸化膜としてはたとえばTiO_2、Ta_2O_5、Al_2O_5、ＰＺＴ、ＳＢＴがある。

【００３１】次に、本発明の第２の実施の形態に係る不揮発性メモリの動作について図１１および図１２を用いて説明する。図１１は、書き込み動作を説明する不揮発性メモリの断面図である。図１２は、消去動作を説明する不揮発性メモリの断面図である。図１１に示すように、メモリセルの書き込み時には、ゲートＧに７～８Ｖ程度、ドレインＤに５Ｖ程度をそれぞれ印加し、ソースＳを接地する。このように電圧を印加し、チャネル熱電子（ＣＨＥ）で電子をドレイン領域側の電荷蓄積層４ｂに注入する。ソース領域側の電荷蓄積層４ａに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記の場合と入れ換えれば良い。一方、メモリセルの消去は、図１２に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ファウラー・ノルドハイム（ＦＮ）型トンネル電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲート電極３が複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳ、ドレインＤはｐ型半導体基板１と同電位とすればよい。また、ｐ型半導体基板１の電

位とは異なる正電圧をドレインＤに印加し、ソースＳを浮遊電位（Floating）とすれば、ドレインＤ側の電荷蓄積層４ａのみから電子を引き抜くことも可能である。ソースＳ側の電荷蓄積層４ｂのみから電子を引き抜く場合にはソースＳに正電圧を印加し、ドレインＤを浮遊電位とすればよい。

【００３２】メモリセルの書き込みは、メモリセルの消去と同様、ＦＮ電流を利用して行うこともできる。ゲートＧとｐ型半導体基板１間に１０Ｖ程度を印加し、ＦＮ電流で電子を電荷蓄積層４ａ、４ｂに注入する。この場合、ゲートＧが共通する複数のメモリセルには同時に電子を注入できる。

【００３３】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【００３４】次に、本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造方法を図１３乃至図１９を用いて説明する。まず図１３に示すように、ｐ型半導体基板１全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ（Jet-Vapor-Deposition）法で行う。ＪＶＤ法についてはたとえば参考文献「T. P. Ma, IEEE Transactions on Electron Devices, Volume 45 Number 3, March 1998 p680」に記載される。第１ゲート絶縁膜１３形成後、ＣＶＤ法によりシリコン酸化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。

【００３５】次に、図１４に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いて、ゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。

【００３６】次に、図１５に示すように、電荷蓄積層形成のための空間１７を形成する。この空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。本発明の第２の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。また、電荷蓄積層形成のための空間１７は、エッチング液を用いたウェットエッチング法に替えてＨＦガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。

【００３７】次に、図１６に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を電荷蓄積層形成のための空間１７が完全に埋め込まれるように堆積する。そして、図１７に示すように、ｐ型半導体基板１全面に対してＲＩＥによる異方性エッチングを行い、電荷蓄積能力の高いシリコン窒化膜で構成された電荷蓄積層４ａおよび４ｂを形成する。

【００３８】次に、図１８に示すように、ｐ型半導体基板１全面に酸化膜１６を形成した後、低不純物濃度のｎ$^-$型拡散層１０を形成する。ｎ$^-$型拡散層１０はイオン注入技術によりゲート電極３をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【００３９】次に、図１９に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｎ$^+$型拡散層１１を形成する。ｎ$^+$型拡散層１１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【００４０】次に、ｐ型半導体基板１の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｐ型半導体基板１を不活性雰囲気中で熱処理することによりゲート電極３およびｎ$^+$型拡散層１１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図１０に示したメモリセル構造が完成する。

【００４１】なお、図示はしないが、図１０のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【００４２】このように、本発明の第２実施の形態では、電荷蓄積層４ａおよび４ｂをゲート電極３の両端の下方に自己整合的に形成することができる。したがって、セルトランジスタのゲート長方向の微細化が可能となる。それにより、大容量、高密度の不揮発性半導体メ

モリを提供できる。また、ビット当りのセル面積は従来と比べてほぼ半減され、大幅に縮小された不揮発性半導体メモリを実現できる。

【００４３】また、電荷蓄積層４ａおよび４ｂのチャネル長方向の幅は第１ゲート絶縁膜１３および第３ゲート絶縁膜１５と第２ゲート絶縁膜１４のエッチング速度差およびエッチング時間の調節によって容易に制御できる。それにより、電荷蓄積層４ａおよび４ｂを対称に配置できる。そして、電荷蓄積層４ａと４ｂは第２ゲート絶縁膜１４によって電気的に完全に分離されるので、電荷蓄積層１４ａと１４ｂ間の相互作用は起こらない。さらに、電荷蓄積層４ａおよび４ｂは、ソース領域、ドレイン領域、ゲート電極３およびチャネル領域から、第１の絶縁膜１３、第３の絶縁膜１５および酸化膜１６によって完全に絶縁されるので、電荷保持特性の優れた不揮発性半導体メモリを提供できる。電荷蓄積層４ａおよび４ｂはゲート電極３の端部からチャネル領域方向に延在して形成され、電荷蓄積層４ａおよび４ｂのうちのチャネル領域側の部分の電荷蓄積状態によってメモリセルの電流伝達特性ほぼ決まる。したがって、この部分のゲート長方向の長さを限界まで縮小すれば、より微細な不揮発性半導体メモリを提供できる。

【００４４】さらに、セル構造は通常のＣＭＯＳ工程で容易に実現可能であるので、既存の製造ラインを使用し低コストで不揮発性半導体メモリを製造できる。

【００４５】（第３の実施の形態）次に、本発明の第３の実施の形態を説明する。本発明の第３の実施の形態は、図１０に示した第２の実施の形態において、第１ゲート絶縁膜１３をシリコン酸化膜、第２ゲート絶縁膜１４をシリコン窒化膜、第３ゲート絶縁膜１５をシリコン酸化膜に置き換えたものである。以下、本発明の第３の実施の形態に係る不揮発性半導体メモリのメモリセルの製造方法を、図１３乃至図１５を参照して説明する。

【００４６】本発明の第３の実施の形態に係る不揮発性半導体メモリのメモリセルは、まず、ｐ型半導体基板１を熱酸化し、１０ｎｍ程度のシリコン酸化膜で構成される第１ゲート絶縁膜１３を形成する。第１ゲート絶縁膜１３形成後、ＪＶＤ法による電荷蓄積能力の低いシリコン窒化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いて、ＣＶＤ法によりシリコン酸化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する（図１３参照）。

【００４７】次に、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続けて、ゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする（図１４参照）。

【００４８】次に、ｐ型半導体基板１を熱酸化し、ｐ型半導体基板１全面に薄いシリコン酸化膜を形成する。その後、電荷蓄積層形成のための空間１７を形成する。この電荷蓄積層形成のための空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。本発明の第３の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン酸化膜で構成し、第２ゲート絶縁膜１４をシリコン窒化膜で構成しているので、エッチング液としてはたとえばリン酸系を用いればよい。なお、シリコン窒化膜１４は熱酸化処理によってはほとんど酸化されないので、第２ゲート絶縁膜の側面には酸化膜は形成されず、このためエッチングの選択性は向上する（図１５参照）。また、電荷蓄積層形成のための空間１７は、エッチング液を用いたウェットエッチング法に替えてCF_4ガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。その後の工程は第２の実施の形態と同一である。

【００４９】（第４の実施の形態）次に、本発明の第４の実施の形態を説明する。図２０は、本発明の第４の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。本発明の第４の実施の形態は、メモリセルをｐ型ＭＯＳトランジスタで構成した例である。図２０に示すように、本発明の第４の実施の形態に係る不揮発性メモリのメモリセル構造では、ｎ型半導体基板１９の表面に第１ゲート絶縁膜１３を介して第２ゲート絶縁膜１４が設けられる。そして、第２ゲート絶縁膜１４の両端には電荷蓄積層４ａ、４ｂが形成される。第２ゲート絶縁膜１４および電荷蓄積層４ａ、４ｂ上には第３ゲート絶縁膜１５を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｎ型半導体基板１９には、チャネル領域に接する低不純物濃度のp^-型拡散層２０と、このp^-型拡散層２０の外側に位置する高不純物濃度のp^+型拡散層２１が設けられる。ゲート電極３およびp^+型拡散層２１それぞれの表面には導電層１２が設けられる。

【００５０】次に、本発明の第４の実施の形態に係る不揮発性メモリの動作について図２１および図２２を用いて説明する。図２１は、書き込み動作を説明する不揮発性メモリの断面図である。図２２は、消去動作を説明する不揮発性メモリの断面図である。図２１に示すように、メモリセルの書き込み時には、ゲートＧに５Ｖ程度、ドレインＤに－５Ｖ程度をそれぞれ印加し、ソースＳを浮遊電位とする。このように電圧を印加し、バンド－バンド間トンネル現象起因の電子にドレイン領域近傍

の電界でエネルギーを与え，ドレイン領域側の電荷蓄積層４ｂに電子を注入する。ソース領域側の電荷蓄積層４ａに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記と入れ替えればよい。一方、メモリセルの消去は、図２２に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ＦＮ電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲートＧが複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳおよびドレインＤはｎ型半導体基板１９と同電位あるいは浮遊電位とする。

【００５１】メモリセルの書き込みは、本発明の第２の実施の形態の場合のようにチャネル熱電子を利用しても行うことが可能である。この場合、ゲートＧに－２．５Ｖ程度、ドレインＤに－５Ｖ程度をそれぞれ印加し、ソースＳを接地する。このように電圧を印加し、チャネル熱電子で電子をドレイン領域側の電荷蓄積層４ｂに注入する。一方、ソース領域側の電荷蓄積層４ａに電子を注入する場合にはドレインＤ、ソースＳそれぞれに印加する電圧を入れ替えればよい。

【００５２】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【００５３】（第５の実施の形態）次に、本発明の第５の実施の形態を説明する。一般に、半導体メモリでは、メモリセルアレイの周辺に周辺回路を配置する。たとえばその周辺回路としてデコーダー、書き込み／消去回路、読み出し回路、アナログ回路、各種のＩ／Ｏ回路、各種のキャパシタ回路等がある。本発明の第５の実施の形態では、これら周辺回路を構成するＭＯＳトランジスタを第２～第４の実施の形態のメモリセルトランジスタの製造工程を用いて同時に製造する例を示すものである。図２３は、本発明の第５の実施の形態に係る不揮発性半導体メモリの周辺回路を構成するＭＯＳトランジスタの構造を示す断面図である。図２３に示すように、本発明の第５の実施の形態によれば、メモリセルトランジスタ（メモリセルＴｒ）以外にゲート絶縁膜の異なる７種類のＭＯＳトランジスタ（Ｔｒ１～Ｔｒ７）を実現できる。なお、図２３のメモリセルトランジスタは図１０に示したメモリセルトランジスタである。また、ＭＯＳトランジスタＴｒ１～Ｔｒ７はすべてｎ型ＭＯＳトランジスタを示している。メモリセルトランジスタのｎ$^-$型拡散層１０およびｎ$^+$型拡散層１１、導電層１２は図面を見易くするために省略してある。ＭＯＳトランジスタＴｒ１～Ｔｒ７についても同様である。

【００５４】次に、図２３に示したＭＯＳトランジスタの製造方法を図２４乃至図３０を用いて説明する。まず図２４に示すように、ｐ型半導体基板１全面にＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。第１ゲート絶縁膜１３形成後、周知の露光技術およびドライエッチング技術によりｐ型半導体基板１上の一部の領域の第１ゲート絶縁膜１３を除去する。そして図２５に示すように、ＣＶＤ法によりシリコン酸化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。第２ゲート絶縁膜１４形成後、露光技術およびドライエッチング技術により一部の領域の第２ゲート絶縁膜１４を除去する。続いて図２６に示すように、ＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。第３ゲート絶縁膜１５形成後、露光技術およびドライエッチング技術により一部の領域の第３ゲート絶縁膜１５を除去する。このようにして第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５のうちの少なくとも１つから構成される７種類のゲート絶縁膜が実現される。

【００５５】次に、図２７に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、複数のゲート電極３を形成する。さらに、ゲート電極３をマスクとしてドライエッチングによりメモリセルトランジスタ、ＭＯＳトランジスタそれぞれのソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を除去する。

【００５６】次に、図２８に示すように、ＭＯＳトランジスタＴｒ１～Ｔｒ７を形成する領域をフォトレジスト２２で覆い、メモリセルトランジスタを形成する領域をウェットエッチングする。エッチング液は第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいものを利用する。このウェットエッチングによりメモリセルトランジスタを形成する領域の第２ゲート絶縁膜１４の端部を選択的にエッチングし、電荷蓄積層形成のための空間１７を形成する。本発明の第５の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。そして、図２９に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を電荷蓄積層形成のための空間

１７が完全に埋め込まれるように堆積する。続いて図３０に示すように、ｐ型半導体基板１全面に対してＲＩＥによる異方性エッチングを行い、メモリセルトランジスタを形成する領域に電荷蓄積能力の高いシリコン窒化膜で構成された電荷蓄積層４ａおよび４ｂを形成する。その後の工程は本発明の第２の実施の形態と同じである。

【００５７】本発明の第５の実施の形態によれば、膜厚が異なるゲート絶縁膜を有する７種類のＭＯＳトランジスタＴｒ１～Ｔｒ７をメモリセルトランジスタと同時に製造できる。それにより、高電圧動作の高耐圧トランジスタから極低電圧動作トランジスタまで多様な動作電圧に対応したＭＯＳトランジスタを提供できる。さらに、ｎ型ＭＯＳトランジスタ、ｐ型ＭＯＳトランジスタ共に実現できる。また、メモリセルトランジスタおよびＭＯＳトランジスタＴｒ１～Ｔｒ７のゲート電極３は同一材料から構成され、同一の露光工程およびドライエッチング工程で形成される。したがって、フォトマスクの位置合わせずれの少ない微細なトランジスタを提供できる。

【００５８】（第６の実施の形態）次に、本発明の第６の実施の形態について説明する。この第６の実施の形態は、電気的に書き込み消去可能な不揮発性メモリと高速に書き込み読み出し可能な揮発性メモリを同一のチップ上に実現する例を示すものである。図３１は、本発明の第６の実施の形態に係る半導体記憶装置に搭載された不揮発性メモリのメモリセル構造を示す断面図、図３２は、本発明の第６の実施の形態に係る半導体記憶装置に搭載された揮発性メモリのメモリセル構造を示す断面図である。図３１の不揮発性メモリと図３２の揮発性メモリとは、同一チップ上に混載されるものである。

【００５９】（Ａ）不揮発性メモリ

図３１に示すように、この第６の実施の形態に係る不揮発性メモリのメモリセルはｎ型ＭＯＳトランジスタで構成される。そして、この不揮発性メモリのメモリセル構造では、ｐ型半導体基板１の主面上に第１ゲート絶縁膜１３を介して第２ゲート絶縁膜１４が設けられる。第２ゲート絶縁膜１４の両端には電荷蓄積層４（４ａ、４ｂ）が形成される。第２ゲート絶縁膜１４および電荷蓄積層４上には第３ゲート絶縁膜１５を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１の主面には、チャネル領域に接する低不純物濃度のｎ$^-$型拡散層１０と、このｎ$^-$型拡散層１０の外側に位置する高不純物濃度のｎ$^+$型拡散層１１が設けられる。ゲート電極３およびｎ$^+$型拡散層１１それぞれの表面には導電層１２が設けられる。

【００６０】本発明の第６の実施の形態に係る不揮発性メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ$^-$型拡散層１０と高不純物濃度のｎ$^+$型拡散層１１.で構成したＬＤＤ構造を有している。そして、ゲート絶縁膜が第１のゲート絶縁膜１３（下層）、第２のゲート絶縁膜１４（中間層）および第３のゲート絶縁膜１５（上層）からなる三層積層膜で構成され、第２ゲート絶縁膜１４の両端部には電荷蓄積層４（４ａ，４ｂ）が形成される。この２つの電荷蓄積層４ａおよび４ｂに電子を蓄積し、その蓄積状態は（１）電荷蓄積層４ａ、４ｂのいずれも電子を蓄積していない状態、（２）電荷蓄積層４ａのみが電子を蓄積している状態、（３）電荷蓄積層４ｂのみが電子を蓄積している状態、（４）電荷蓄積層４ａ、４ｂ共に電子を蓄積している状態、の４つの状態をとり得る。この２つの電荷蓄積層４ａおよび４ｂに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。また、このメモリセル構造では電荷蓄積層４はチャネル領域端部の上方に位置するので、チャネル領域中央部のしきい値電圧はチャネル領域の不純物濃度のみで決まり、電荷蓄積層４の電子の蓄積状態に依存しない。したがって、電荷蓄積層４の電子の過不足による過消去（over-erase）は防止され、それにより過消去に起因するリーク不良、プログラム不良、読み出し不良等は生じ得ない。また、ソース領域とドレイン領域間のリーク電流はゲート電圧のみで抑制でき、高信頼性の不揮発性メモリを実現できる。電荷蓄積層４はＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第１ゲート絶縁膜１３、第３ゲート絶縁膜１５をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度なので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細化のみならず周辺高電圧動作素子の微細化も可能となる。

【００６１】本発明の第６の実施の形態に係る不揮発性メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｎ$^-$型拡散層１０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を構成してもよい。第２ゲート絶縁膜１４は電荷蓄積層４ａ－４ｂ間のリークを防止するが、たとえばシリコン酸化膜で構成することができる。また、第２ゲート絶縁膜１４に高誘電率を有する金属酸化膜を用いれば、チャネル領域中央の電流伝達特性を向上できる。金属酸化膜としてはたとえばTiO_2、Ta_2O_5、Al_2O_5、ＰＺＴ、

ＳＢＴがある。

【００６２】次に、本発明の第６の実施の形態に係る不揮発性半導体メモリの動作について図３３および図３４を用いて説明する。図３３は、書き込み動作を説明する不揮発性メモリの断面図である。図３４は、消去動作を説明する不揮発性メモリの断面図である。図３３に示すように、メモリセルの書き込み時には、ゲートＧに７～８Ｖ程度、ドレインＤに５Ｖ程度をそれぞれ印加し、ソースＳを接地する。このように電圧を印加し、チャネル熱電子（ＣＨＥ）で電子をドレイン領域側の電荷蓄積層４ｂに注入する。ソース領域側の電荷蓄積層４ｂに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記と入れ替えればよい。一方、メモリセルの消去は、図３４に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ファウラー・ノルドハイム（ＦＮ）型トンネル電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲートＧが複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳ、ドレインＤはｐ型半導体基板１と同電位とすればよい。また、ｐ型半導体基板１の電位とは異なる正電圧をドレイン電極に印加し、ソース電極を浮遊電位（Floating）とすれば、ドレイン電極側の電荷蓄積層４ｂのみから電子を引き抜くことも可能である。ソース電極側の電荷蓄積層４ａのみから電子を引き抜く場合にはソース電極に正電圧を印加し、ドレイン電極を浮遊電位とすればよい。

【００６３】メモリセルの書き込みは、メモリセルの消去と同様、ＦＮ電流を利用して行うこともできる。ゲートＧとｐ型半導体基板１間に１０Ｖ程度を印加し、ＦＮ電流で電子を電荷蓄積層４ａ、４ｂに注入する。この場合、ゲートＧが共通する複数のメモリセルには同時に電子を注入できる。

【００６４】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【００６５】（Ｂ）揮発性メモリ

図３２に示すように、本発明の第６の実施の形態に係る揮発性メモリのメモリセルはｎ型ＭＯＳトランジスタで構成される。この揮発性メモリのメモリセル構造では、ｐ型半導体基板１の主面上に、図３１の第２ゲート絶縁膜１４が直接配置される。そして、第２ゲート絶縁膜１４の両端には、図３１の不揮発性メモリと同様、電荷蓄積層４（４ｃ、４ｄ）が形成されるが、この電荷蓄積層４ｃおよび４ｄがトンネル絶縁膜２３を介してｐ型半導体基板１の主面上に配置される点が図３１の不揮発性メモリとは異なる。第２ゲート絶縁膜１４および電荷蓄積層４上には第３ゲート絶縁膜１５を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１の主面には、チャネル領域に接する低不純物濃度のｎ$^-$型拡散層１０と、このｎ$^-$型拡散層１０の外側に位置する高不純物濃度のｎ$^+$型拡散層１１が設けられる。ゲート電極３およびｎ$^+$型拡散層１１それぞれの表面には導電層１２が設けられる。

【００６６】本発明の第６の実施の形態に係る揮発性メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ$^-$型拡散層１０と高不純物濃度のｎ$^+$型拡散層１１で構成したＬＤＤ構造を有している。そして、ゲート絶縁膜が第２のゲート絶縁膜１４、トンネル絶縁膜２３および第３のゲート絶縁膜１５で構成され、第２ゲート絶縁膜１４の両端部には電荷蓄積層４が形成される。この２つの電荷蓄積層４ｃおよび４ｄに電子を蓄積し、その蓄積状態は（１）電荷蓄積層４ｃ、４ｄのいずれも電子を蓄積していない状態、（２）電荷蓄積層４ｃのみが電子を蓄積している状態、（３）電荷蓄積層４ｄのみが電子を蓄積している状態、（４）電荷蓄積層４ｃ、４ｄ共に電子を蓄積している状態、の４つの状態をとり得る。この２つの電荷蓄積層４ｃおよび４ｄに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。また、このメモリセル構造では電荷蓄積層４はチャネル領域端部の上方に位置するので、チャネル領域中央部のしきい値電圧はチャネル領域の不純物濃度のみで決まり、電荷蓄積層４の電子の蓄積状態に依存しない。したがって、電荷蓄積層４の電子の過不足による過消去（over-erase）は防止され、それにより過消去に起因するリーク不良、プログラム不良、読み出し不良等は生じ得ない。また、ソース領域とドレイン領域間のリーク電流はゲート電圧のみで抑制でき、高信頼性の揮発性メモリを実現できる。電荷蓄積層４はＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第３ゲート絶縁膜１５をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度な

ので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細化のみならず周辺高電圧動作素子の微細化も可能となる。

【００６７】本発明の第６の実施の形態に係る揮発性メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｎ⁻型拡散層１０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を構成してもよい。第２ゲート絶縁膜１４は電荷蓄積層４ｃ－４ｄ間のリークを防止するが、たとえばシリコン酸化膜で構成することができる。また、第２ゲート絶縁膜１４に高誘電率を有する金属酸化膜を用いれば、チャネル領域中央の電流伝達特性を向上できる。金属酸化膜としてはたとえばTiO_2、Ta_2O_5、Al_2O_5、ＰＺＴ、ＳＢＴがある。

【００６８】本発明の第６の実施の形態に係る揮発性メモリでは、電荷蓄積層４ｃおよび４ｄの下部にトンネル絶縁膜２３を配置している。トンネル絶縁膜２３は直接トンネリング可能な膜厚を有する薄膜のシリコン酸化膜で構成され、ダイナミックＲＡＭに要求される１００ｎｓ以下での高速書き込み読み出しを可能とする。トンネル絶縁膜２３をシリコン酸化膜で構成した場合、その膜厚は３ｎｍ以下とすれば良い。また、３ｎｍ以下のシリコン窒化膜で構成すれば、シリコン酸化膜換算膜厚が１．５ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。トンネル絶縁膜２３を介する漏れ電流によって電荷蓄積層４に蓄積された電子は徐々に減っていくので、実際は長期間のデータ保持は困難である。しかし、通常のダイナミックＲＡＭのリフレッシュ期間内で十分再書き込み可能であり、ダイナミックＲＡＭとしての動作には全く問題ないと考える。このことは、C. H-J. Wann らによって1995IEDM digest p. 867に示されている。

【００６９】メモリセルの読み込みはソース電極とドレイン電極の間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ｃ、４ｄの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソース電極、ドレイン電極のどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ｃおよび４ｄの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【００７０】さらに、本発明の第６の実施の形態に係る揮発性メモリは、電荷蓄積層４ｃおよび４ｄに電荷を注入しなければ、通常のＭＯＳトランジスタとして動作させることが可能である。

【００７１】（Ｃ）不揮発性および揮発性混載メモリの製造方法

次に、本発明の第６の実施の形態に係る不揮発性メモリおよび揮発性メモリのメモリセルの製造方法を図３５乃至図４３および図４４乃至図５２を用いて説明する。図３５乃至図４３は、本発明の第６の実施の形態に係る不揮発性メモリの製造方法を示す断面図、図４４乃至図５２は、本発明の第６の実施の形態に係る揮発性メモリの製造方法を示す断面図である。

【００７２】まず図３５および図４４に示すように、ｐ型半導体基板１全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。第１ゲート絶縁膜１３形成後、図３５の不揮発性メモリ形成領域をたとえばフォトレジストで覆い、図４４の揮発性メモリ形成領域の第１ゲート絶縁膜１３のみをたとえば加熱燐酸溶液を用いたウェットエッチング法により除去する。したがって、第１のゲート絶縁膜１３は図３５の不揮発性メモリ形成領域のみに形成される。電荷蓄積能力の小さいシリコン窒化膜の堆積は、たとえばＪＶＤ法で行う。

【００７３】次に、図３６および図４５に示すように、ＣＶＤ法によりシリコン酸化膜をｐ型半導体基板１全面に堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。結局、図３６の不揮発性メモリ形成領域には第１、第２および第３のゲート絶縁膜１３，１４，１５が形成され、図４５の揮発性メモリ形成領域には第２および第３ゲート絶縁膜１４，１５が形成される。

【００７４】次に、図３７および図４６に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いてゲート電極３をマスクとして、図３７の不揮発性メモリ形成領域では、ソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。一方、図４６の揮発性メモリ形成領域では、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。

【００７５】次に、図３８および図４７に示すように、電荷蓄積層形成のための空間１７を形成する。この空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。図３８の不揮発性メモリ形成領域の電荷蓄積層形成のための空間１７および図４７の揮発性メモリ形成領域の電荷蓄積層形成のための空間１７は同時に形成される。本発明の第６の実施の形態では、第１ゲート酸化膜１３およ

び第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。また、この空間１７は、エッチング液を用いたウェットエッチング法に替えてＨＦガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。

【００７６】次に、図３９および図４８に示すように、ｐ型半導体基板１全面をたとえばＲＴＯ法により酸化し、直接トンネル可能なシリコン酸化膜から成るトンネル絶縁膜２３を形成する。

【００７７】次に、図４０および図４９に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を電荷蓄積層形成のための空間１７が完全に埋め込まれるように堆積する。そして、図４１および図５０に示すように、ｐ型半導体基板１全面に対してＲＩＥによる異方性エッチングを行い、電荷蓄積能力の高いシリコン窒化膜で構成された電荷蓄積層４（４ａ，４ｂ，４ｃ，４ｄ）を同時に形成する。

【００７８】次に、図４２および図５１に示すように、ｐ型半導体基板１全面に酸化膜１６を形成した後、低不純物濃度のｎ$^-$型拡散層１０を形成する。ｎ$^-$型拡散層１０はイオン注入技術によりゲート電極３をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【００７９】次に、図４３および図５２に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｎ$^+$型拡散層１１を形成する。ｎ$^+$型拡散層１１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【００８０】そして、ｐ型半導体基板１の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｐ型半導体基板１を不活性雰囲気中で熱処理することによりゲート電極３およびｎ$^+$型拡散層１１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図３１に示した不揮発性メモリおよび図３２に示した揮発性メモリのメモリセル構造が完成する。

【００８１】なお、図示はしないが、図３１および図３２のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリおよび揮発性メモリを搭載した半導体装置が完成する。

【００８２】このように本発明の第６実施の形態では、電荷蓄積層４（４ａ，４ｂ，４ｃ，４ｄ）をゲート電極３の両端の下方に自己整合的に形成することができる。したがって、図３１および図３２のメモリセルトランジスタのゲート長方向の微細化が可能となる。それにより、大容量、高密度の不揮発性メモリおよび揮発性メモリを提供できる。また、ビット当りのセル面積は従来と比べてほぼ半減され、大幅に縮小された不揮発性メモリおよび揮発性メモリを実現できる。

【００８３】電荷蓄積層４のチャネル長方向の幅は、ｐ型半導体基板１、第１ゲート絶縁膜１３および第３ゲート絶縁膜１５と第２ゲート絶縁膜１４のエッチング速度差およびエッチング時間の調節によって容易に制御できる。それにより、電荷蓄積層４を対称に配置できる。そして、電荷蓄積層４間は第２ゲート絶縁膜１４によって電気的に完全に分離されるので、電荷蓄積層４間の相互作用は起こらない。さらに、電荷蓄積層４は、ソース領域、ドレイン領域、ゲート電極３およびチャネル領域からは、第１の絶縁膜１３、トンネル絶縁膜２３、第３の絶縁膜１５および酸化膜１６によって完全に絶縁されるので、電荷保持特性の優れた不揮発性メモリおよび揮発性メモリを提供できる。電荷蓄積層４はゲート電極３の端部からチャネル領域方向に延在して形成され、電荷蓄積層４のうちのチャネル領域側の部分の電荷蓄積状態によってメモリセルの電流伝達特性はほぼ決まる。したがって、この部分のゲート長方向の長さを限界まで縮小すれば、より微細な不揮発性メモリおよび揮発性メモリを提供できる。

【００８４】セル構造は通常のＣＭＯＳ工程で容易に実現可能であるので、既存の製造ラインを使用し低コストで不揮発性メモリおよび揮発性メモリを製造できる。

【００８５】さらに、上記の不揮発性メモリと揮発性メモリは、その製造工程の大部分が共通化されているので、低コストでかつ短い製造工期で、不揮発性メモリと揮発性メモリを混載した半導体装置を製造することができる。

【００８６】なお、本発明の第６の実施の形態では、第１ゲート絶縁膜１３をシリコン窒化膜、第２ゲート絶縁膜１４をシリコン酸化膜、第３ゲート絶縁膜１５をシリコン窒化膜で構成しているが、第１ゲート絶縁膜１３をシリコン酸化膜、第２ゲート絶縁膜１４をシリコン窒化膜、第３ゲート絶縁膜１５をシリコン酸化膜で構成しても良い。この場合たとえば、第１ゲート絶縁膜１３はｐ型半導体基板１を熱酸化した１０ｎｍ程度のシリコン酸化膜で構成する。第２ゲート絶縁膜１４はＪＶＤ法により堆積した５～１０ｎｍ程度の電荷蓄積能力の低いシリコン窒化膜で構成する。第３ゲート絶縁膜１５はＣＶＤ法により堆積した１０ｎｍ程度のシリコン酸化膜で構成すれば良い。また、電荷蓄積層形成のための空間１７の形成は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン酸化膜で構成し、第２ゲート絶縁膜１４をシリコン窒化膜で構成しているので、エッチング液としてはたとえばリン酸系を用いればよい。

【００８７】（第７の実施の形態）次に、本発明の第７の実施の形態を説明する。この第７の実施の形態は、上記の第６の実施の形態と同様、電気的に書き込み消去可能な不揮発性メモリと高速に書き込み読み出し可能な揮発性メモリを同一のチップ上に実現する例を示すものである。図５３は、本発明の第７の実施の形態に係る半導体記憶装置に搭載された不揮発性メモリのメモリセル構造を示す断面図、図５４は、本発明の第７の実施の形態に係る半導体記憶装置に搭載された揮発性メモリのメモリセル構造を示す断面図である。図５３の不揮発性メモリと図５４の揮発性メモリとは、同一チップ上に混載されるものである。図５３に示す不揮発性メモリについては上記の第６の実施の形態と同様であるので、ここではその説明を省略する。

【００８８】図５４に示すように、この第７の実施の形態に係る揮発性メモリのメモリセルはｎ型ＭＯＳトランジスタで構成される。そして、この揮発性メモリのメモリセル構造では、ｐ型半導体基板１の主面上にトンネル絶縁膜２３を介して電荷蓄積層４ｅが配置される。電荷蓄積層４ｅ上には第４ゲート絶縁膜２４を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１の主面には、チャネル領域に接する低不純物濃度のｎ$^{-}$型拡散層１０と、このｎ$^{-}$型拡散層１０の外側に位置する高不純物濃度のｎ$^{+}$型拡散層１１が設けられる。ゲート電極３およびｎ$^{+}$型拡散層１１それぞれの表面には導電層１２が設けられる。

【００８９】本発明の第７の実施の形態に係る揮発性メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ$^{-}$型拡散層１０と高不純物濃度のｎ$^{+}$型拡散層１１で構成したＬＤＤ構造を有している。そして、ゲート絶縁膜がトンネル絶縁膜２３および第４のゲート絶縁膜２１から成る積層構造で構成され、トンネル絶縁膜２３と第４ゲート絶縁膜２４の間には電荷蓄積層４ｅが配置される。この電荷蓄積層４ｅに電子を蓄積し、この電荷蓄積層４ｅに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“０”、“１”に対応させる。電荷蓄積層４ｅはＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第４ゲート絶縁膜２４をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度なので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細化のみならず周辺高電圧動作素子の微細化も可能となる。

【００９０】本発明の第７の実施の形態に係る揮発性メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｎ$^{-}$型拡散層１０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を構成してもよい。

【００９１】本発明の第７の実施の形態に係る揮発性メモリにおいて、電荷蓄積層４ｅの下部にトンネル絶縁膜２３を配置している。トンネル絶縁膜２３は直接トンネリング可能な膜厚を有する薄膜のシリコン酸化膜で構成され、ダイナミックＲＡＭに要求される１００ｎｓ以下での高速書き込み読み出しが可能となる。トンネル絶縁膜２３をシリコン酸化膜で構成した場合、その膜厚は３ｎｍ以下とすれば良い。また、３ｎｍ以下のシリコン窒化膜で構成すれば、シリコン酸化膜換算膜厚が１．５ｎｍ程度の非常に薄いトンネル絶縁膜２３を安定して実現できる。

【００９２】さらに、本発明の第７の実施の形態に係る揮発性メモリは、電荷蓄積層４ｅに電荷を注入しなければ、通常のＭＯＳトランジスタとして動作させることも可能である。

【００９３】次に、本発明の第７の実施の形態に係る不揮発性メモリおよび揮発性メモリのメモリセルの製造方法を図５５乃至図６２および図６３乃至図７０を用いて説明する。図５５乃至図６２は、本発明の第７の実施の形態に係る不揮発性メモリの製造方法を示す断面図、図６３乃至図７０は、本発明の第７の実施の形態に係る揮発性メモリの製造方法を示す断面図である。

【００９４】まず図５５および図６３に示すように、ｐ型半導体基板１全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ法で行う。第１ゲート絶縁膜１３形成後、ＣＶＤ法によりシリコン酸化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。

【００９５】次に、図５６および図６４に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、図５６の不揮発性メモリ形成領域では、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いてゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜

１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。図６４の揮発性メモリ形成領域では、多結晶シリコン膜、第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５はすべて除去され、ｐ型半導体基板１表面が露出する。

【００９６】次に、図５７に示すように、不揮発性メモリ形成領域では、電荷蓄積層形成のための空間１７を形成する。この電荷蓄積層形成のための空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。本発明の第７の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。また、電荷蓄積層系形成のための空間１７は、エッチング液を用いたウェットエッチング法に替えてＨＦガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。一方、図６５に示すように、揮発性メモリ形成領域では、ｐ型半導体基板１の表面が露出したままである。

【００９７】次に、図５８および図６６に示すように、ｐ型半導体基板１全面をたとえばＲＴＯ法によりに直接トンネル可能なシリコン酸化膜から成るトンネル絶縁膜２３を形成する。トンネル絶縁膜２３形成後、ｐ型半導体基板１全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を堆積する。この時、電荷蓄積層形成のための空間１７がシリコン窒化膜１８によって完全に埋め込まれる。そして、図５９に示すように、不揮発性メモリ形成領域では、ｐ型半導体基板１全面に対してＲＩＥによる異方性エッチングを行い、電荷蓄積能力の高いシリコン窒化膜１８で構成された電荷蓄積層４（４ａ，４ｂ）を形成する。その際、図６７の揮発性メモリ形成領域は、フォトレジストで覆われており、シリコン窒化膜１８はエッチングされない。

【００９８】シリコン窒化膜１８のエッチング終了後、ｐ型半導体基板１全面にシリコン酸化膜を堆積し、第４ゲート絶縁膜２４を形成する。ここで、図５９の不揮発性メモリ形成領域の第４ゲート絶縁膜２４は除去される。その除去は、図６７の揮発性メモリ形成領域をフォトレジストで覆い、図５９の不揮発性メモリ形成領域に堆積された第４ゲート絶縁膜２４をエッチングすることで行われる。

【００９９】次に、図６８に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積する。そして、露光技術およびエッチング技術によりその多結晶シリコン膜をパターニングし、ゲート電極３ａを形成する。続いてゲート電極３ａをエッチングマスクとして、ソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面のトンネル絶縁膜２３、電荷蓄積層４ｅおよび第４ゲート絶縁膜２４を自己整合的にドライエッチングする。一方、不揮発性メモリ形成領域では、図６０に示すように、多結晶シリコン膜をすべて除去しても良いし、ゲート電極３に合わせてパターニングし、新たなゲート電極を形成しても良い。

【０１００】次に、図６１および図６９に示すように、ｐ型半導体基板１全面に酸化膜１６を形成した後、低不純物濃度のｎ$^{-}$型拡散層１０を形成する。ｎ$^{-}$型拡散層１０はイオン注入技術によりゲート電極３をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１０１】次に、図６２および図７０に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｎ$^{+}$型拡散層１１を形成する。ｎ$^{+}$型拡散層１１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１０２】次に、ｐ型半導体基板１の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｐ型半導体基板１を不活性雰囲気中で熱処理することによりゲート電極３およびｎ$^{+}$型拡散層１１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図５３に示した不揮発性メモリおよび図５４に示した揮発性メモリのメモリセル構造が完成する。

【０１０３】図示はしないが、図５３および図５４のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルおよび揮発性メモリセルが完成する。

【０１０４】本発明の第７の実施の形態では、第１ゲート絶縁膜１３をシリコン窒化膜、第２ゲート絶縁膜１４をシリコン酸化膜、第３ゲート絶縁膜１５をシリコン窒化膜で構成しているが、第１ゲート絶縁膜１３をシリコン酸化膜、第２ゲート絶縁膜１４をシリコン窒化膜、第３ゲート絶縁膜１５をシリコン酸化膜で構成しても良い。この場合たとえば、第１ゲート絶縁膜１３はｐ型半導体基板１を熱酸化した１０ｎｍ程度のシリコン酸化膜で構成する。第２ゲート絶縁膜１４はＪＶＤ法により堆積した５～１０ｎｍ程度の電荷蓄積能力の低いシリコン窒化膜で構成する。第３ゲート絶縁膜１５はＣＶＤ法により堆積した１０ｎｍ程度のシリコン酸化膜で構成すれば良い。また、電荷蓄積層形成のための空間１７の形成

は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン酸化膜で構成し、第２ゲート絶縁膜１４をシリコン窒化膜で構成しているので、エッチング液としてはたとえばリン酸系を用いればよい。

【０１０５】本発明の第６および第７の実施の形態では、不揮発性メモリおよび揮発性メモリのメモリセルは共にｎ型ＭＯＳトランジスタで構成される例について説明したが、反対導電型のｐ型ＭＯＳトランジスタのメモリセルであっても良いことはもちろんである。この場合には、上記の説明において、適宜、基板や拡散層の導電タイプを反対のものに読み替えれば良い。

【０１０６】（第８の実施の形態）次に、本発明の第８の実施の形態について説明する。上記の第１乃至第７の実施の形態では、電荷蓄積層の構造は電子注入効率の向上に直接には寄与しない。フローティングゲート構造の不揮発性半導体メモリでは、チャネル部分に段差を設けて、電子注入効率を向上させる試みが提案されている（S.Ogura, 1998IEDM,p987, 米国特許番号第５７８０３４１号）。しかしながら、この提案では、フローティングゲート構造を採用するため、酸化膜中の欠陥やリークサイトに対しては弱い。また、段差構造形成時に発生しうる欠陥に対しても、十分な信頼性を得られないおそれがある。本発明の第８の実施の形態は、簡単なプロセスで、電子注入効率を向上させることができるものである。

【０１０７】図７１は、本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。この第８の実施の形態は、メモリセルのチャネル領域に段差や傾斜を設けることで、書き込み時における電子注入効率の向上を図るものである。図７１に示すように、このメモリセルはｎ型ＭＯＳトランジスタで構成される。そして、この第８の実施の形態に係るメモリセルの構造では、ｐ型半導体基板１の表面に第１ゲート絶縁膜１３を介して第２ゲート絶縁膜１４が設けられる。第２ゲート絶縁膜１４の両端には電荷蓄積層４ａ、４ｂが形成される。第２ゲート絶縁膜１４および電荷蓄積層４ａ、４ｂ上には第３ゲート絶縁膜１５を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１には、チャネル領域に接する低不純物濃度のｎ$^-$型拡散層１０と、このｎ$^-$型拡散層１０の外側に位置する高不純物濃度のｎ$^+$型拡散層１１が設けられる。ゲート電極３およびｎ$^+$型拡散層１１それぞれの表面には導電層１２が設けられる。

【０１０８】さらに、本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセル構造では、チャネル領域２５に段差２６が設けられる。この段差２６により、ｐ型半導体基板１内の電子の散乱方向に電荷蓄積層４が位置することになる。したがって、書き込み時における電子の注入効率が向上する。

【０１０９】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ$^-$型拡散層１０と高不純物濃度のｎ$^+$型拡散層１１で構成したＬＤＤ構造を有している。そして、ゲート絶縁膜が第１ゲート絶縁膜１３（下層）、第２ゲート絶縁膜１４（中間層）および第３ゲート絶縁膜１５（上層）からなる３層積層膜で構成され、第２ゲート絶縁膜１４の両端部には電荷蓄積層４ａおよび４ｂが形成される。この２つの電荷蓄積層４ａおよび４ｂに電子を蓄積し、その蓄積状態は（１）電荷蓄積層４ａ、４ｂのいずれも電子を蓄積していない状態、（２）電荷蓄積層４ａのみが電子を蓄積している状態、（３）電荷蓄積層４ｂのみが電子を蓄積している状態、（４）電荷蓄積層４ａ、４ｂ共に電子を蓄積している状態、の４つの状態をとり得る。この２つの電荷蓄積層４ａおよび４ｂに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。また、このメモリセル構造では電荷蓄積層４ａ、４ｂはチャネル領域端部の上方に位置するので、チャネル領域中央部のしきい値電圧はチャネル領域の不純物濃度のみで決まり、電荷蓄積層４ａ、４ｂの電子の蓄積状態に依存しない。したがって、電荷蓄積層４ａ、４ｂの電子の過不足による過消去（over-erase）は防止され、それにより過消去に起因するリーク不良、プログラム不良、読み出し不良等は生じ得ない。また、ソース領域とドレイン領域間のリーク電流はゲート電圧のみで抑制でき、高信頼性の不揮発性半導体メモリを実現できる。電荷蓄積層４ａおよび４ｂはＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第１ゲート絶縁膜１３、第３ゲート絶縁膜１５をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度なので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細化のみならず周辺高電圧動作素子の微細化も可能となる。

【０１１０】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｎ$^-$型拡散層１０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を

構成してもよい。第２ゲート絶縁膜１４は電荷蓄積層４ａ－４ｂ間のリークを防止するが、たとえばシリコン酸化膜で構成することができる。また、第２ゲート絶縁膜１４に高誘電率を有する金属酸化膜を用いれば、チャネル領域中央の電流伝達特性を向上できる。金属酸化膜としてはたとえばTiO_2、Ta_2O_5、Al_2O_5、ＰＺＴ、ＳＢＴがある。

【０１１１】本発明の第８の実施の形態では、ソース側、ドレイン側の両方に、段差２６を設けたが、どちらか一方のみに設けても良い。特に、１ビット分の情報を記憶するメモリでは、一方のみあれば十分である。

【０１１２】次に、本発明の第８の実施の形態に係る不揮発性メモリの動作について図７２および図７３を用いて説明する。図７２は、書き込み動作を説明する不揮発性メモリの断面図である。図７３は、消去動作を説明する不揮発性メモリの断面図である。図７２に示すように、メモリセルの書き込み時には、ゲートＧに６～８Ｖ程度、ドレインＤに４～５Ｖ程度をそれぞれ印加し、ソースＳを接地する。このように電圧を印加し、チャネル熱電子（ＣＨＥ）で電子をドレイン領域側の電荷蓄積層４ｂに注入する。チャネル領域２５に段差２６を設けたことで、電子の散乱方向に電荷蓄積層４ｂに位置している。このために、電荷蓄積層４ｂに対する電子の注入効率が向上し、注入速度の高速化、印加電圧の低減化、を図ることができる。ソース領域側の電荷蓄積層４ａに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記の場合と入れ換えれば良い。一方、メモリセルの消去は、図７３に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ファウラー・ノルドハイム（ＦＮ）型トンネル電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲート電極３が複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳ、ドレインＤはｐ型半導体基板１と同電位とすればよい。また、ｐ型半導体基板１の電位とは異なる正電圧をドレインＤに印加し、ソースＳを浮遊電位（Floating）とすれば、ドレインＤ側の電荷蓄積層４ａのみから電子を引き抜くことも可能である。ソースＳ側の電荷蓄積層４ｂのみから電子を引き抜く場合にはソースＳに正電圧を印加し、ドレインＤを浮遊電位とすればよい。

【０１１３】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【０１１４】次に、本発明の第８の実施の形態に係る不揮発性メモリのメモリセルの製造方法を図７４乃至図８２を用いて説明する。まず図７４に示すように、チャネル領域２５が形成される領域を覆うフォトレジストパターン２７を、ｐ型半導体基板１上に形成する。そして、図７５に示すように、たとえばＲＩＥ法によって、ｐ型半導体基板１をエッチングすることで、段差２６を形成する。

【０１１５】次に、図７６に示すように、ｐ型半導体基板１全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ法で行う。第１ゲート絶縁膜１３形成後、ＣＶＤ法によりシリコン酸化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。

【０１１６】次に、図７７に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いて、ゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。

【０１１７】次に、図７８に示すように、電荷蓄積層形成のための空間１７を形成する。この空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。本発明の第８の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。また、電荷蓄積層形成のための空間１７は、エッチング液を用いたウェットエッチング法に替えてＨＦガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。

【０１１８】次に、図７９に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を電荷蓄積層形成のための空間１７が完全に埋め込まれるように堆積する。そして、図８０に示すように、ｐ型半導体基板１全面に対してＲＩＥによる異方性エッチングを行い、電荷蓄積能力の高いシリコン窒化膜で構成された電荷蓄積層４ａおよび４ｂを形成する。

【０１１９】次に、図８１に示すように、ｐ型半導体基

板１全面に酸化膜１６を形成した後、低不純物濃度のｎ⁻型拡散層１０を形成する。ｎ⁻型拡散層１０はイオン注入技術によりゲート電極３をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１２０】次に、図８２に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｎ⁺型拡散層１１を形成する。ｎ⁺型拡散層１１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１２１】次に、ｐ型半導体基板１の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｐ型半導体基板１を不活性雰囲気中で熱処理することによりゲート電極３およびｎ⁺型拡散層１１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図７１に示したメモリセル構造が完成する。

【０１２２】なお、図示はしないが、図７１のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【０１２３】このように、本発明の第８実施の形態では、電荷蓄積層４ａおよび４ｂをゲート電極３の両端の下方に自己整合的に形成することができる。したがって、セルトランジスタのゲート長方向の微細化が可能となる。それにより、大容量、高密度の不揮発性半導体メモリを提供できる。また、ビット当りのセル面積は従来と比べてほぼ半減され、大幅に縮小された不揮発性半導体メモリを実現できる。

【０１２４】また、電荷蓄積層４ａおよび４ｂのチャネル長方向の幅は第１ゲート絶縁膜１３および第３ゲート絶縁膜１５と第２ゲート絶縁膜１４のエッチング速度差およびエッチング時間の調節によって容易に制御できる。それにより、電荷蓄積層４ａおよび４ｂを対称に配置できる。そして、電荷蓄積層４ａと４ｂは第２ゲート絶縁膜１４によって電気的に完全に分離されるので、電荷蓄積層１４ａと１４ｂ間の相互作用は起こらない。さらに、電荷蓄積層４ａおよび４ｂはソース領域、ドレイン領域、ゲート電極３およびチャネル領域からは第１の絶縁膜１３および第３の絶縁膜１５、酸化膜１６によって完全に絶縁されるので、電荷保持特性の優れた不揮発性半導体メモリを提供できる。電荷蓄積層４ａおよび４ｂはゲート電極３の端部からチャネル領域方向に延在して形成され、電荷蓄積層４ａおよび４ｂのうちのチャネル領域側の部分の電荷蓄積状態によってメモリセルの電

流伝達特性ほぼ決まる。したがって、この部分のゲート長方向の長さを限界まで縮小すれば、より微細な不揮発性半導体メモリを提供できる。

【０１２５】さらに、セル構造は通常のＣＭＯＳ工程で容易に実現可能であるので、既存の製造ラインを使用し低コストで不揮発性半導体メモリを製造できる。

【０１２６】そして、本発明の第８の実施の形態では、書き込み時の電子注入効率を向上させることができる。このため、書き込み速度の高速化、書き込み時の印加電圧の低減化を図ることができる。

【０１２７】（第９の実施の形態）次に、本発明の第９の実施の形態について説明する。本発明の第９の実施の形態は、上記の第８の実施の形態において、図７１の電荷蓄積層４ａと電荷蓄積層４ｂ間に配置された第２の絶縁膜１４を不要とし、２つの電荷蓄積層４ａおよび４ｂを一体化させた構成を採っている。図８３は、本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。図８３に示すように、このメモリセル構造は、上記の第８の実施の形態の電荷蓄積層４ａ、４ｂ、および第２の絶縁膜１４に換えて、電荷蓄積層４ｆを、配置したものである。

【０１２８】次に、本発明の第９の実施の形態に係る不揮発性メモリのメモリセルの製造方法を図８４乃至図８９を用いて説明する。上記の第８の実施の形態と同様、まず図８４に示すように、チャネル領域２５が形成される領域を覆うフォトレジストパターン２７を、ｐ型半導体基板１上に形成する。そして、図８５に示すように、たとえばＲＩＥ法によって、ｐ型半導体基板１をエッチングすることで、段差２６を形成する。

【０１２９】次に、図８６に示すように、ｐ型半導体基板１全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ法で行う。第１ゲート絶縁膜１３形成後、ＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を５～１０ｎｍ程度形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。

【０１３０】次に、図８７に示すように、ｐ型半導体基板１全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いて、ゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｐ型半導体基板１の表面の第１ゲート絶縁膜１３、シリコン窒化膜１８および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。ここで、電荷蓄積層４ｆが形成される。

【０１３１】次に、図８８に示すように、ｐ型半導体基板１全面に酸化膜１６を形成した後、低不純物濃度のｎ

－型拡散層１０を形成する。ｎ－型拡散層１０はイオン注入技術によりゲート電極３をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１３２】次に、図８９に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｎ＋型拡散層１１を形成する。ｎ＋型拡散層１１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｎ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１３３】次に、ｐ型半導体基板１の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｐ型半導体基板１を不活性雰囲気中で熱処理することによりゲート電極３およびｎ＋型拡散層１１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図８３に示したメモリセル構造が完成する。

【０１３４】なお、図示はしないが、図８３のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【０１３５】（第１０の実施の形態）次に、本発明の第１０の実施の形態について説明する。図９０は、本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。上記の第８および第９の実施の形態では、チャネル領域を半導体基板に対して凸状態とすることで、チャネル領域の両端に段差を設けたが、この第１０の実施の形態では、チャネル領域を半導体基板に対して凹状態とすることで、チャネル領域に段差を設けるものである。そして、この第１０の実施の形態も、メモリセルのチャネル領域に段差や傾斜を設けることで、書き込み時における電子注入効率の向上を図るものである。

【０１３６】図９０に示すように、このメモリセルはｐ型ＭＯＳトランジスタで構成される。そして、この第１０の実施の形態に係るメモリセルの構造では、ｎ型半導体基板１９の表面に第１ゲート絶縁膜１３を介して第２ゲート絶縁膜１４が設けられる。第２ゲート絶縁膜１４の両端には電荷蓄積層４ａ、４ｂが形成される。第２ゲート絶縁膜１４および電荷蓄積層４ａ、４ｂ上には第３ゲート絶縁膜１５を介してゲート電極３が設けられる。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｎ型半導体基板１９には、チャネル領域に接する低不純物濃度のｐ－型拡散層２０と、このｐ－型拡散層２０の外側に位置する高不純物濃度のｐ＋型拡散層２１が設けられる。ゲート電極３およびｐ＋型拡散層２１それぞれの表面には導電層１２が設けられる。

【０１３７】さらに、本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセル構造では、チャネル領域２５に段差２６が設けられる。この段差２６により、ｐ型半導体基板１内の電子の散乱方向に電荷蓄積層４が位置することになる。したがって、書き込み時における電子の注入効率が向上する。

【０１３８】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｐ－型拡散層２０と高不純物濃度のｐ＋型拡散層２１で構成したＬＤＤ構造を有している。そして、ゲート絶縁膜が第１ゲート絶縁膜１３（下層）、第２ゲート絶縁膜１４（中間層）および第３ゲート絶縁膜１５（上層）からなる３層積層膜で構成され、第２ゲート絶縁膜１４の両端部には電荷蓄積層４ａおよび４ｂが形成される。この２つの電荷蓄積層４ａおよび４ｂに電子を蓄積し、その蓄積状態は（１）電荷蓄積層４ａ、４ｂのいずれも電子を蓄積していない状態、（２）電荷蓄積層４ａのみが電子を蓄積している状態、（３）電荷蓄積層４ｂのみが電子を蓄積している状態、（４）電荷蓄積層４ａ、４ｂ共に電子を蓄積している状態、の４つの状態をとり得る。この２つの電荷蓄積層４ａおよび４ｂに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。また、このメモリセル構造では電荷蓄積層４ａ、４ｂはチャネル領域端部の上方に位置するので、チャネル領域中央部のしきい値電圧はチャネル領域の不純物濃度のみで決まり、電荷蓄積層４ａ、４ｂの電子の蓄積状態に依存しない。したがって、電荷蓄積層４ａ、４ｂの電子の過不足による過消去（over-erase）は防止され、それにより過消去に起因するリーク不良、プログラム不良、読み出し不良等は生じ得ない。また、ソース領域とドレイン領域間のリーク電流はゲート電圧のみで抑制でき、高信頼性の不揮発性半導体メモリを実現できる。電荷蓄積層４ａおよび４ｂはＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第１ゲート絶縁膜１３、第３ゲート絶縁膜１５をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度なので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細

化のみならず周辺高電圧動作素子の微細化も可能となる。

【０１３９】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｐ－型拡散層２０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を構成してもよい。第２ゲート絶縁膜１４は電荷蓄積層４ａ－４ｂ間のリークを防止するが、たとえばシリコン酸化膜で構成することができる。また、第２ゲート絶縁膜１４に高誘電率を有する金属酸化膜を用いれば、チャネル領域中央の電流伝達特性を向上できる。金属酸化膜としてはたとえばTiO_2、Ta_2O_5、Al_2O_5、ＰＺＴ、ＳＢＴがある。

【０１４０】本発明の第１０の実施の形態では、ソース側、ドレイン側の両方に、段差２６を設けたが、どちらか一方のみに設けても良い。特に、１ビット分の情報を記憶するメモリでは、一方のみあれば十分である。

【０１４１】次に、本発明の第１０の実施の形態に係る不揮発性メモリの動作について図９１および図９２を用いて説明する。図９１は、書き込み動作を説明する不揮発性メモリの断面図である。図９２は、消去動作を説明する不揮発性メモリの断面図である。図９１に示すように、メモリセルの書き込み時には、ゲートＧに５Ｖ程度、ドレインＤに－５Ｖ程度をそれぞれ印加し、ソースＳを浮遊電位とする。このように電圧を印加し、バンドーバンド間トンネル現象起因の電子にドレイン近傍の電界でエネルギーを与え、ドレイン領域側の電荷蓄積層４ｂに注入する。チャネル領域２５に段差２６を設けたことで、電子の注入方向に電荷蓄積層４ｂが位置している。このために、電荷蓄積層４ｂに対する電子の注入効率が向上し、注入速度の高速化、印加電圧の低減化、を図ることができる。ソース領域側の電荷蓄積層４ａに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記の場合と入れ換えれば良い。一方、メモリセルの消去は、図９２に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ファウラー・ノルドハイム（ＦＮ）型トンネル電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲート電極３が複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳ、ドレインＤはｎ型半導体基板１９と同電位とすればよい。また、ｐ型半導体基板１の電位とは異なる正電圧をドレインＤに印加し、ソースＳを浮遊電位（Floating）とすれば、ドレインＤ側の電荷蓄積層４ａのみから電子を引き抜くことも可能である。ソースＳ側の電荷蓄積層４ｂのみから電子を引き抜く場合にはソースＳに正電圧を印加し、ドレインＤを浮遊電位とすればよい。

【０１４２】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【０１４３】次に、本発明の第１０の実施の形態に係る不揮発性メモリのメモリセルの製造方法を図９３乃至図１０１を用いて説明する。まず図９３に示すように、チャネル領域２５が形成される領域以外を覆うフォトレジストパターン２７を、ｎ型半導体基板１９上に形成する。そして、図９４に示すように、たとえばＲＩＥ法によって、ｎ型半導体基板１９をエッチングすることで、段差２６を形成する。

【０１４４】次に、図９５に示すように、ｎ型半導体基板１９全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ法で行う。第１ゲート絶縁膜１３形成後、ＣＶＤ法によりシリコン酸化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。

【０１４５】次に、図９６に示すように、ｎ型半導体基板１９全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いて、ゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｎ型半導体基板１９の表面の第１ゲート絶縁膜１３、第２ゲート絶縁膜１４および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。

【０１４６】次に、図９７に示すように、電荷蓄積層形成のための空間１７を形成する。この空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。本発明の第１０の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。また、電荷蓄積層形成のための空間１７は、エッチング液を用いたウェットエッチング法に替えてＨＦガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。

【０１４７】次に、図９８に示すように、ｎ型半導体基

板１９全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を電荷蓄積層形成のための空間１７が完全に埋め込まれるように堆積する。そして、図９９に示すように、ｎ型半導体基板１９全面に対してＲＩＥによる異方性エッチングを行い、電荷蓄積能力の高いシリコン窒化膜で構成された電荷蓄積層４ａおよび４ｂを形成する。

【０１４８】次に、図１００に示すように、ｎ型半導体基板１９全面に酸化膜１６を形成した後、低不純物濃度のｐ⁻型拡散層２０を形成する。ｐ⁻型拡散層２０はイオン注入技術によりゲート電極３をマスクとしてｐ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１４９】次に、図１０１に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｐ⁺型拡散層２１を形成する。ｐ⁺型拡散層２１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｐ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１５０】次に、ｎ型半導体基板１９の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｎ型半導体基板１９を不活性雰囲気中で熱処理することによりゲート電極３およびｐ⁺型拡散層２１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図９０に示したメモリセル構造が完成する。

【０１５１】なお、図示はしないが、図９０のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【０１５２】このように、本発明の第１０実施の形態では、電荷蓄積層４ａおよび４ｂをゲート電極３の両端の下方に自己整合的に形成することができる。したがって、セルトランジスタのゲート長方向の微細化が可能となる。それにより、大容量、高密度の不揮発性半導体メモリを提供できる。また、ビット当りのセル面積は従来と比べてほぼ半減され、大幅に縮小された不揮発性半導体メモリを実現できる。

【０１５３】また、電荷蓄積層４ａおよび４ｂのチャネル長方向の幅は第１ゲート絶縁膜１３および第３ゲート絶縁膜１５と第２ゲート絶縁膜１４のエッチング速度差およびエッチング時間の調節によって容易に制御できる。それにより、電荷蓄積層４ａおよび４ｂを対称に配置できる。そして、電荷蓄積層４ａと４ｂは第２ゲート絶縁膜１４によって電気的に完全に分離されるので、電荷蓄積層１４ａと１４ｂ間の相互作用は起こらない。さ

らに、電荷蓄積層４ａおよび４ｂはソース領域、ドレイン領域、ゲート電極３およびチャネル領域からは第１の絶縁膜１３および第３の絶縁膜１５、酸化膜１６によって完全に絶縁されるので、電荷保持特性の優れた不揮発性半導体メモリを提供できる。電荷蓄積層４ａおよび４ｂはゲート電極３の端部からチャネル領域方向に延在して形成され、電荷蓄積層４ａおよび４ｂのうちのチャネル領域側の部分の電荷蓄積状態によってメモリセルの電流伝達特性はほぼ決まる。したがって、この部分のゲート長方向の長さを限界まで縮小すれば、より微細な不揮発性半導体メモリを提供できる。

【０１５４】さらに、セル構造は通常のＣＭＯＳ工程で容易に実現可能であるので、既存の製造ラインを使用し低コストで不揮発性半導体メモリを製造できる。

【０１５５】そして、本発明の第１０の実施の形態では、書き込み時の電子注入効率を向上させることができる。このため、書き込み速度の高速化、書き込み時の印加電圧の低減化を図ることができる。

【０１５６】（第１１の実施の形態）次に、本発明の第１１の実施の形態について説明する。本発明の第１１の実施の形態は、上記の第１０の実施の形態において、図９０の電荷蓄積層４ａと電荷蓄積層４ｂ間に配置された第２の絶縁膜１４を不要とし、２つの電荷蓄積層４ａおよび４ｂを一体化させた構成を採っている。図１０２は、本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。図１０２に示すように、このメモリセル構造は、上記の第１０の実施の形態の電荷蓄積層４ａ、４ｂ、および第２の絶縁膜１４に換えて、電荷蓄積層４ｆを、配置したものである。

【０１５７】次に、本発明の第１１の実施の形態に係る不揮発性メモリのメモリセルの製造方法を図１０３乃至図１０８を用いて説明する。上記の第１０の実施の形態と同様、まず図１０３に示すように、チャネル領域２５が形成される領域以外を覆うフォトレジストパターン２７を、ｎ型半導体基板１９上に形成する。そして、図１０４に示すように、たとえばＲＩＥ法によって、ｎ型半導体基板１９をエッチングすることで、段差２６を形成する。

【０１５８】次に、図１０５に示すように、ｎ型半導体基板１９全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ法で行う。第１ゲート絶縁膜１３形成後、ＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を５～１０ｎｍ程度形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。

【０１５９】次に、図１０６に示すように、ｎ型半導体基板１９全面にＬＰＣＶＤ法によりｎ型またはｐ型不純

物をドープした５０～２５０ｎｍ程度の多結晶シリコン膜を堆積した後、露光技術およびエッチング技術によりパターニングし、ゲート電極３を形成する。続いて、ゲート電極３をマスクとしてソース領域およびドレイン領域を形成する領域のｎ型半導体基板１９の表面の第１ゲート絶縁膜１３、シリコン窒化膜１８および第３ゲート絶縁膜１５を自己整合的にドライエッチングする。ここで、電荷蓄積層４ｆが形成される。

【０１６０】次に、図１０７に示すように、ｎ型半導体基板１９全面に酸化膜１６を形成した後、低不純物濃度のｐ－型拡散層２０を形成する。ｐ－型拡散層２０はイオン注入技術によりゲート電極３をマスクとしてｐ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１６１】次に、図１０８に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高不純物濃度のｐ＋型拡散層２１を形成する。ｐ＋型拡散層２１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｐ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１６２】次に、ｎ型半導体基板１９の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｎ型半導体基板１９を不活性雰囲気中で熱処理することによりゲート電極３およびｐ＋型拡散層２１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図１０２に示したメモリセル構造が完成する。

【０１６３】なお、図示はしないが、図１０２のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【０１６４】（第１２の実施の形態）次に、本発明の第１２の実施の形態について説明する。図１０９は、本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの構造を示す断面図である。上記の第１０の実施の形態では、ゲート電極３のパターニングに露光技術およびエッチング技術を用いたが、この第１２の実施の形態では、ゲート電極３のパターニングに化学的機械的研磨法を用いる例である。

【０１６５】次に、本発明の第１２の実施の形態に係る不揮発性メモリのメモリセルの製造方法を図１１０乃至図１１８を用いて説明する。まず図１１０に示すように、チャネル領域２５が形成される領域以外を覆うフォトレジストパターン２７を、ｎ型半導体基板１９上に形成する。そして、図１１１に示すように、たとえばＲＩＥ法によって、ｎ型半導体基板１９をエッチングすることで、段差２６を形成する。

【０１６６】次に、図１１２に示すように、ｎ型半導体基板１９全面に電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第１ゲート絶縁膜１３を形成する。電荷蓄積能力の小さいシリコン窒化膜の堆積はたとえばＪＶＤ法で行う。第１ゲート絶縁膜１３形成後、ＣＶＤ法によりシリコン酸化膜を堆積し、５～１０ｎｍ程度の第２ゲート絶縁膜１４を形成する。続いてＪＶＤ法により電荷蓄積能力の小さいシリコン窒化膜を堆積し、１０ｎｍ程度の第３ゲート絶縁膜１５を形成する。さらに、ｎ型半導体基板１９全面にＬＰＣＶＤ法によりｎ型またはｐ型不純物をドープした５０～５００ｎｍ程度の多結晶シリコン膜２８を堆積する。

【０１６７】次に、図１１３に示すように、化学的機械的研磨方法によって、多結晶シリコン膜１９の埋め込みを行なうことで、ゲート電極３を形成する。なお、通常、ｎ型半導体基板１９上に残存する第１のゲート絶縁膜１３、第２のゲート絶縁膜１４および第３のゲート絶縁膜１５を、たとえばウェットエッチングにより除去される。

【０１６８】次に、図１１４に示すように、電荷蓄積層形成のための空間１７を形成する。この空間１７は、第１ゲート酸化膜１３および第３ゲート絶縁膜１５よりも第２ゲート絶縁膜１４のエッチング速度が大きいエッチング液を用いて第２ゲート絶縁膜１４の端部を選択的にウェットエッチングすることで形成する。本発明の第１２の実施の形態では、第１ゲート酸化膜１３および第３ゲート絶縁膜１５をシリコン窒化膜で構成し、第２ゲート絶縁膜１４をシリコン酸化膜で構成しているので、エッチング液としてはたとえばフッ酸系を用いればよい。また、電荷蓄積層形成のための空間１７は、エッチング液を用いたウェットエッチング法に替えてＨＦガスを含むガスを用いたプラズマドライエッチング法で形成してもよい。

【０１６９】次に、図１１５に示すように、ｎ型半導体基板１９全面にＬＰＣＶＤ法により電荷蓄積能力の高いシリコン窒化膜１８を電荷蓄積層形成のための空間１７が完全に埋め込まれるように堆積する。そして、図１１６に示すように、ｎ型半導体基板１９全面に対してＲＩＥによる異方性エッチングを行い、電荷蓄積能力の高いシリコン窒化膜で構成された電荷蓄積層４ａおよび４ｂを形成する。

【０１７０】次に、図１１７に示すように、ｎ型半導体基板１９全面に酸化膜１６を形成した後、低不純物濃度のｐ－型拡散層２０を形成する。ｐ－型拡散層２０はイオン注入技術によりゲート電極３をマスクとしてｐ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１７１】次に、図１１８に示すように、ゲート電極３の側壁にサイドウォールスペーサ９を形成した後、高

不純物濃度のｐ＋型拡散層２１を形成する。ｐ＋型拡散層２１はイオン注入技術によりゲート電極３およびサイドウォールスペーサ９をマスクとしてｐ型不純物を注入し、その後の熱処理によって注入した不純物を活性化することで形成する。

【０１７２】次に、ｎ型半導体基板１９の全面にＣＶＤ法またはスパッタ法によってタングステン、チタン、コバルトなどの高融点金属膜を堆積し、続いて、ｎ型半導体基板１９を不活性雰囲気中で熱処理することによりゲート電極３およびｐ＋型拡散層２１それぞれの表面に高融点金属シリサイドで構成される導電層１２を形成する。導電層１２形成後、上記以外の領域に残った未反応の高融点金属を除去すれば、図１０９に示したメモリセル構造が完成する。

【０１７３】なお、図示はしないが、図１０９のメモリセル構造完成後、層間絶縁膜形成工程、コンタクトホール形成工程、配線形成工程、パッシベイション膜形成工程等の通常のＣＭＯＳ製造工程を順次経て、最終的な不揮発性メモリセルが完成する。

【０１７４】（第１３の実施の形態）次に、本発明の第１３の実施の形態について説明する。上記の第１乃至第１２の実施の形態では、メモリセル以外のトランジスタの高速化に対する十分な検討はなされていなかった。一方、高速ＣＭＯＳトランジスタの構造として、ゲート電極とソース・ドレイン拡散層間に凹上のノッチを形成することで、ゲート電極と拡散層間の容量を低減し、ロジックゲートを高速化する試みがなされている（T. Ghani et al., IEDM99, p415）。この第１３の実施の形態は、この構造を不揮発性半導体メモリに利用することで、メモリ機能を有しない通常のトランジスタと不揮発性半導体メモリとを混載する半導体装置の大幅な高速化を可能とするものである。

【０１７５】図１１９は、本発明の第１３の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。このメモリセルはｎ型ＭＯＳトランジスタで構成される。本発明の第１３の実施の形態に係る不揮発性半導体メモリのメモリセル構造では、ｐ型半導体基板１の表面に第１ゲート絶縁膜１３を介してゲート電極３が設けられる。ゲート電極３の両端には凹部が設けられ、各凹部内には、電荷蓄積層４（４ａ、４ｂ）が形成される。電荷蓄積層４とゲート電極３との間には、酸化膜３０が形成されている。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の下部のｐ型半導体基板１の主面には、チャネル領域に接する低不純物濃度のｎ－型拡散層１０と、このｎ－型拡散層１０の外側に位置する高不純物濃度のｎ＋型拡散層１１が設けられる。ゲート電極３およびｎ＋型拡散層１１それぞれの表面には導電層１２が設けられる。

【０１７６】本発明の第１３の実施の形態に係る不揮発性メモリのメモリセルは、ソース領域およびドレイン領域を低不純物濃度のｎ－型拡散層１０と高不純物濃度のｎ＋型拡散層１１で構成したＬＤＤ構造を有している。そして、ゲート電極３の両端部には電荷蓄積層４（４ａ，４ｂ）が形成される。この２つの電荷蓄積層４ａおよび４ｂに電子を蓄積し、その蓄積状態は（１）電荷蓄積層４ａ、４ｂのいずれも電子を蓄積していない状態、（２）電荷蓄積層４ａのみが電子を蓄積している状態、（３）電荷蓄積層４ｂのみが電子を蓄積している状態、（４）電荷蓄積層４ａ、４ｂ共に電子を蓄積している状態、の４つの状態をとり得る。この２つの電荷蓄積層４ａおよび４ｂに保持された電子の有無によって生じるしきい値電圧の変化分を記憶情報の“００”、“０１”、“１０”、“１１”に対応させる。また、このメモリセル構造では電荷蓄積層４はチャネル領域端部の上方に位置するので、チャネル領域中央部のしきい値電圧はチャネル領域の不純物濃度のみで決まり、電荷蓄積層４の電子の蓄積状態に依存しない。したがって、電荷蓄積層４の電子の過不足による過消去（over-erase）は防止され、それにより過消去に起因するリーク不良、プログラム不良、読み出し不良等は生じ得ない。また、ソース領域とドレイン領域間のリーク電流はゲート電圧のみで抑制でき、高信頼性の不揮発性メモリを実現できる。電荷蓄積層４はＣＶＤ法による電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。さらに、第１ゲート絶縁膜１３をシリコン酸化膜（SiO_2膜）の２倍程度の誘電率を有するシリコン窒化膜（Si_3N_4膜）で構成すれば、シリコン酸化膜換算膜厚が４ｎｍ～１１ｎｍ程度の非常に薄いゲート絶縁膜を安定して実現できる。たとえばシリコン酸化膜換算膜厚が５ｎｍのシリコン窒化膜の実質膜厚は１０ｎｍ程度なので、直接トンネル（ＤＴ）注入も誘起されない。したがって、電子の注入抽出動作時の電圧は低電圧化され、メモリセルの微細化のみならず周辺高電圧動作素子の微細化も可能となる。

【０１７７】本発明の第１３の実施の形態に係る不揮発性メモリのメモリセルでは、ソース領域およびドレイン領域の耐圧向上の目的でｎ－型拡散層１０を設け、ＬＤＤ構造を構成しているが、シングルドレイン構造、ダブルドレイン構造でソース領域およびドレイン領域を構成してもよい。

【０１７８】次に、本発明の第１３の実施の形態に係る不揮発性メモリの動作について図１２０および図１２１を用いて説明する。図１２０は、書き込み動作を説明する不揮発性メモリの断面図である。図１２１は、消去動作を説明する不揮発性メモリの断面図である。図１２０および図１２１のメモリセルはｎ型ＭＯＳトランジスタ

で構成される。図１２０に示すように、メモリセルの書き込み時には、ゲートＧに６～８Ｖ程度、ドレインＤに４～５Ｖ程度をそれぞれ印加し、ソースＳを接地する。このように電圧を印加し、チャネル熱電子（ＣＨＥ）で電子をドレイン領域側の電荷蓄積層４ｂに注入する。ソース領域側の電荷蓄積層４ｂに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記と入れ替えればよい。一方、メモリセルの消去は、図１２１に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ファウラー・ノルドハイム（ＦＮ）型トンネル電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲートＧが複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳ、ドレインＤはｐ型半導体基板１と同電位とすればよい。また、ｐ型半導体基板１の電位とは異なる正電圧をドレイン電極に印加し、ソース電極を浮遊電位（Floating）とすれば、ドレイン電極側の電荷蓄積層４ｂのみから電子を引き抜くことも可能である。ソース電極側の電荷蓄積層４ａのみから電子を引き抜く場合にはソース電極に正電圧を印加し、ドレイン電極を浮遊電位とすればよい。

【０１７９】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【０１８０】次に、ｐ型ＭＯＳトランジスタで構成される、本発明の第１３の実施の形態に係る不揮発性メモリの動作について図１２２および図１２３を用いて説明する。図１２２は、書き込み動作を説明する不揮発性メモリの断面図である。図１２３は、消去動作を説明する不揮発性メモリの断面図である。図１２２および図１２３のメモリセルはｐ型ＭＯＳトランジスタで構成される。図１２２に示すように、メモリセルの書き込み時には、ゲートＧに５Ｖ程度、ドレインＤに－５Ｖ程度をそれぞれ印加し、ソースＳを浮遊電位とする。このように電圧を印加し、バンドーバンド間トンネル現象起因の電子にドレイン領域近傍の電界でエネルギーを与え，ドレイン領域側の電荷蓄積層４ｂに電子を注入する。ソース領域側の電荷蓄積層４ａに電子を注入する場合には、ドレインＤ、ソースＳそれぞれに印加する電圧を上記と入れ替えればよい。一方、メモリセルの消去は、図１２３に示すように、ゲートＧに負電圧（～－５Ｖ）を印加し、ＦＮ電流を利用して電荷蓄積層４ａ、４ｂから電子を引き抜くことで行われる。また、ゲートＧが複数のメモリセルで共有されている場合には、それらのメモリセルから同時に電子を引き抜くことができる。この場合、ソースＳおよびドレインＤはｎ型半導体基板１９と同電位あるいは浮遊電位とする。

【０１８１】また図示はしないが、メモリセルの読み出しは、ソースＳとドレインＤの間を流れる読み出し電流を検知することで行われる。電荷蓄積層４ａ、４ｂの蓄積状態によってソース領域、ドレイン領域近傍の電流伝達特性（チャネルコンダクタンス）が変調することを利用するものである。ソースＳ、ドレインＤのどちらにバイアスするかは電流伝達特性の変調が顕著に現れる方を選択すればよい。電荷蓄積層４ａおよび４ｂの４つの蓄積状態によって４つの異なる電流伝達特性が得られ、それにより１つのセルで２ビット分の情報を記憶できる。

【０１８２】本発明の第１３の実施の形態では、図１２４に示すように、メモリ機能を有しない通常のＭＯＳトランジスタも実現可能である。なぜならば、このＭＯＳトランジスタでは、電荷蓄積層４は、ソース・ドレイン領域１０，１１上のみに配置され、チャネル領域上には配置されていない。このため、このＭＯＳトランジスタの伝導特性は、電荷蓄積層４の電荷の保持状態に、何ら影響を受けることはないからである。さらに、ゲート電極３の凹部の存在によって、ゲートーソース・ドレイン間の寄生容量が低減され、ＭＯＳトランジスタの高速動作が可能となるという有利な点も有している。

【０１８３】（第１４の実施の形態）次に、本発明の第１４の実施の形態について説明する。この第１４の実施の形態は、上記の第１３の実施の形態において、電荷蓄積層４とサイドウォールスペーサ９を一体化させた構成となっている。図１２５は、本発明の第１４の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。このメモリセルはｎ型ＭＯＳトランジスタで構成される。本発明の第１４の実施の形態に係る不揮発性半導体メモリのメモリセル構造では、ｐ型半導体基板１の表面に第１ゲート絶縁膜１３を介してゲート電極３が設けられる。ゲート電極３の両端には凹部が設けられ、各凹部内には、電荷蓄積層４（４ａ、４ｂ）が形成される。電荷蓄積層４とゲート電極３との間には、酸化膜３０が形成されている。ゲート電極３の側面には酸化膜１６を介してサイドウォールスペーサ９が設けられ、このサイドウォールスペーサ９の一部が電荷蓄積層４を構成する。サイドウォールスペーサ９の下部のｐ型半導体基板１の主面には、チャネル領域に接する低不純物濃度のｎ$^{-}$型拡散層１０と、このｎ$^{-}$型拡散層１０の外側に位置する高不純物濃度のｎ$^{+}$型拡散層１１が設けられる。ゲート電極３およびｎ$^{+}$型拡散層１１それぞれの表面には導電層１２が設けられる。

【０１８４】本発明の第１４の実施の形態では、サイドウォールスペーサ９および電荷蓄積層４は、ＣＶＤ法に

よる電荷蓄積能力の高いシリコン窒化膜で構成すればよい。シリコン窒化膜の離散的な電荷捕獲準位に電子を蓄積することで、下部絶縁膜の膜質に影響を受け難い電荷保持特性を得ることができるからである。また、シリコン膜、多結晶シリコン膜で構成すれば安価に製造できる。

【０１８５】本発明の第１４の実施の形態では、上記の第１３の実施の形態と同様、図１２６に示すような、通常のＭＯＳトランジスタも実現できる。

【０１８６】

【発明の効果】本発明によれば、簡単なセル構造で複数ビット分の情報を記憶することができる不揮発性半導体記憶装置の構造を実現できる。

【０１８７】本発明によれば、簡単な製造プロセスで複数ビット分の情報を記憶する不揮発性半導体記憶装置を製造する不揮発性半導体記憶装置の製造方法を実現できる。

【０１８８】本発明によれば、簡単なセル構造で電気的に書き込み消去可能な不揮発性メモリと高速書き込み読み出し可能な揮発性メモリを混載した半導体記憶装置の構造を実現できる。

【０１８９】本発明によれば、簡単な製造プロセスで電気的に書き込み消去可能な不揮発性メモリと高速書き込み読み出し可能な揮発性メモリを混載した半導体記憶装置の製造方法を実現できる。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図２】本発明の第１の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図３】本発明の第１の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図４】本発明の第１の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図５】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図６】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図７】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図８】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図９】本発明の第１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１０】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図１１】本発明の第２の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図１２】本発明の第２の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図１３】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１４】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１５】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１６】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１７】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１８】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１９】本発明の第２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図２０】本発明の第４の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図２１】本発明の第４の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図２２】本発明の第４の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図２３】本発明の第５の実施の形態に係る不揮発性メモリの周辺回路を構成するＭＯＳトランジスタの構造を示す断面図である。

【図２４】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図２５】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図２６】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図２７】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図２８】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図２９】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図３０】図２３のＭＯＳトランジスタの製造工程を示す断面図である。

【図３１】本発明の第６の実施の形態に係る半導体記憶装置に搭載された不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図３２】本発明の第６の実施の形態に係る半導体記憶装置に搭載された揮発性半導体メモリのメモリセル構造を示す断面図である。

【図３３】本発明の第６の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。
【図３４】本発明の第６の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。
【図３５】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図３６】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図３７】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図３８】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図３９】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４０】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４１】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４２】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４３】本発明の第６の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４４】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４５】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４６】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図４７】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
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【図５０】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５１】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５２】本発明の第６の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５３】本発明の第７の実施の形態に係る半導体記憶装置に搭載された不揮発性半導体メモリのメモリセル構造を示す断面図である。
【図５４】本発明の第７の実施の形態に係る半導体記憶装置に搭載された揮発性半導体メモリのメモリセル構造を示す断面図である。
【図５５】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５６】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５７】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５８】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図５９】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６０】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６１】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６２】本発明の第７の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６３】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６４】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６５】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６６】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６７】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６８】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図６９】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７０】本発明の第７の実施の形態に係る揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７１】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。
【図７２】本発明の第８の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。
【図７３】本発明の第８の実施の形態に係る不揮発性半

導体メモリの動作を説明する断面図である。
【図７４】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７５】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７６】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７７】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７８】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図７９】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８０】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８１】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８２】本発明の第８の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８３】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。
【図８４】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８５】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８６】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８７】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８８】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図８９】本発明の第９の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９０】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。
【図９１】本発明の第１０の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。
【図９２】本発明の第１０の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。
【図９３】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９４】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９５】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９６】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９７】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９８】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図９９】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１００】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０１】本発明の第１０の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０２】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。
【図１０３】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０４】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０５】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０６】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０７】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。
【図１０８】本発明の第１１の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図で

ある。

【図１０９】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図１１０】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１１】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１２】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１３】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１４】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１５】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１６】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１７】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１８】本発明の第１２の実施の形態に係る不揮発性半導体メモリのメモリセルの製造工程を示す断面図である。

【図１１９】本発明の第１３の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図１２０】ｎ型ＭＯＳトランジスタで構成された、本発明の第１３の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図１２１】ｎ型ＭＯＳトランジスタで構成された、本発明の第１３の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図１２２】ｐ型ＭＯＳトランジスタで構成された、本発明の第１３の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図１２３】ｐ型ＭＯＳトランジスタで構成された、本発明の第１３の実施の形態に係る不揮発性半導体メモリの動作を説明する断面図である。

【図１２４】本発明の第１３の実施の形態に係る不揮発性半導体メモリのメモリセルと同一のゲート構造を有するＭＯＳトランジスタの構造を示す断面図である。

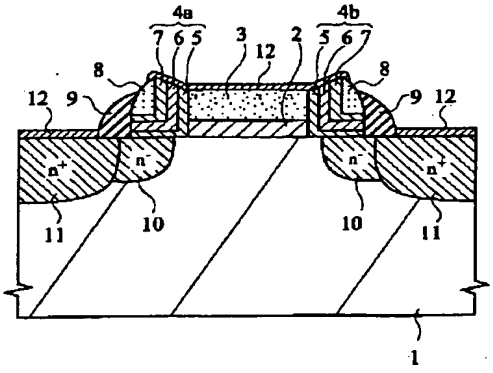
【図１２５】本発明の第１４の実施の形態に係る不揮発性半導体メモリのメモリセル構造を示す断面図である。

【図１２６】本発明の第１４の実施の形態に係る不揮発性半導体メモリのメモリセルと同一のゲート構造を有するＭＯＳトランジスタの構造を示す断面図である。

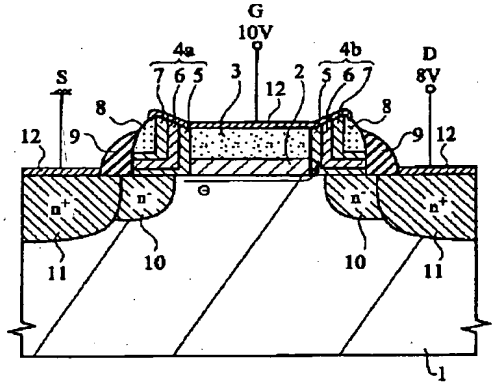
【符号の説明】

１　ｐ型半導体基板
２　ゲート絶縁膜
３　ゲート電極（第１ゲート電極）
４　電荷蓄積層
５　第１酸化膜
６　窒化膜
７　第２酸化膜
８　第２ゲート電極
９　サイドウォールスペーサ
１０　ｎ$^-$型拡散層
１１　ｎ$^+$型拡散層
１２　導電層
１３　第１ゲート絶縁膜
１４　第２ゲート絶縁膜
１５　第３ゲート絶縁膜
１６　酸化膜
１７　電荷蓄積層形成のための空間
１８　シリコン窒化膜
１９　ｎ型半導体基板
２０　Ｐ$^-$型拡散層
２１　ｐ$^+$型拡散層
２２，２７　フォトレジスト（フォトレジストパターン）
２３　トンネル絶縁膜
２４　第４ゲート絶縁膜
２５　チャネル領域
２６　段差
２８　多結晶シリコン膜

【図１】



【図２】



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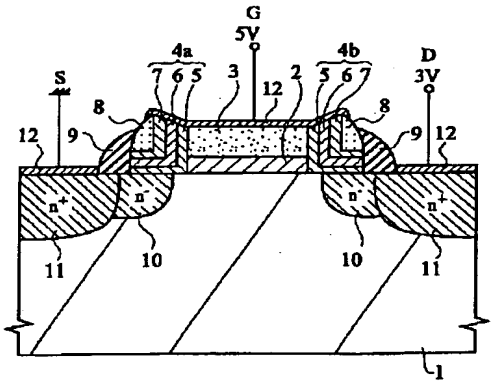

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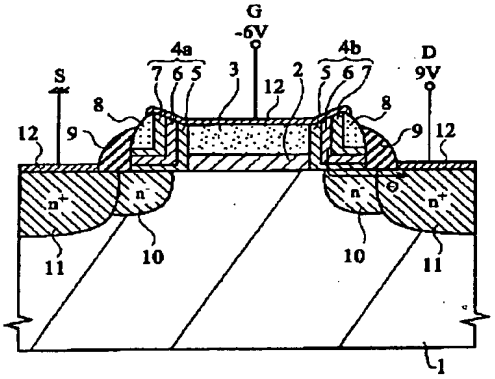

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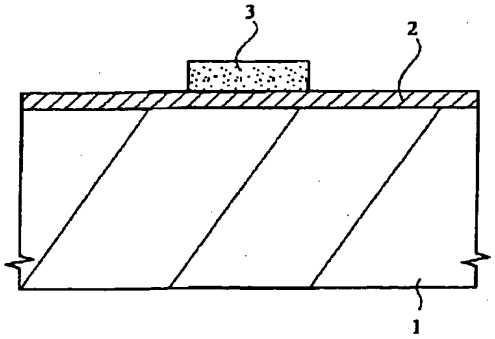

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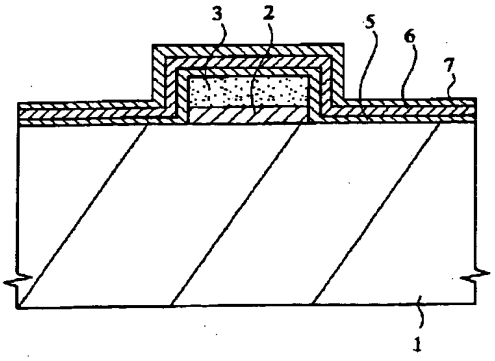

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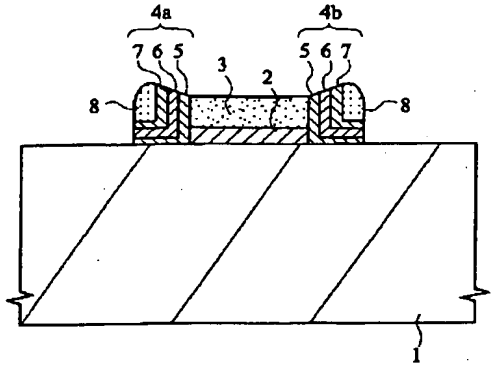

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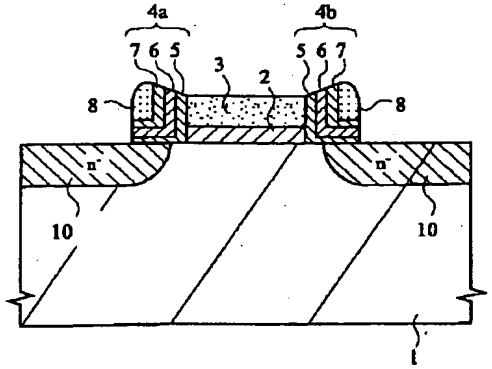

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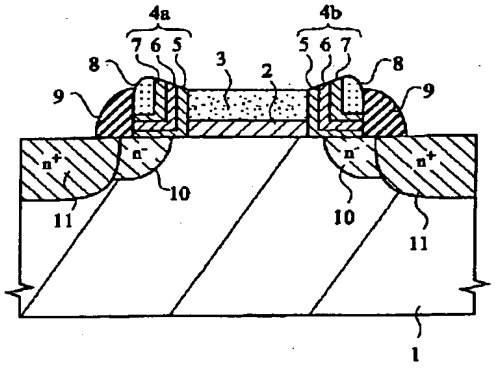
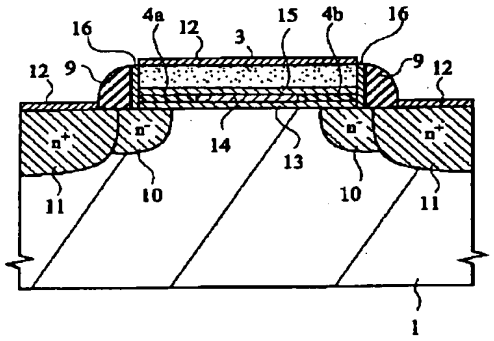
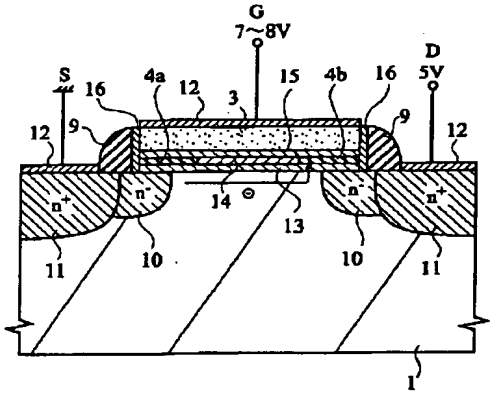


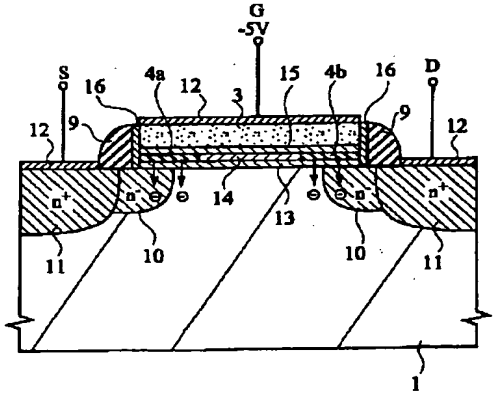
【図１０】



【図１１】



【図１２】



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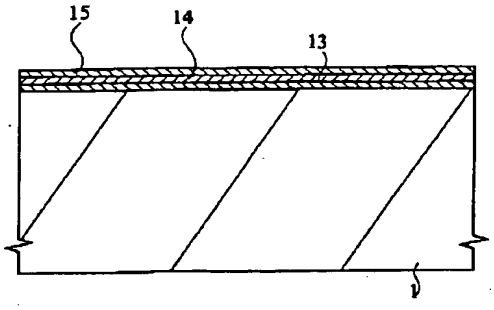

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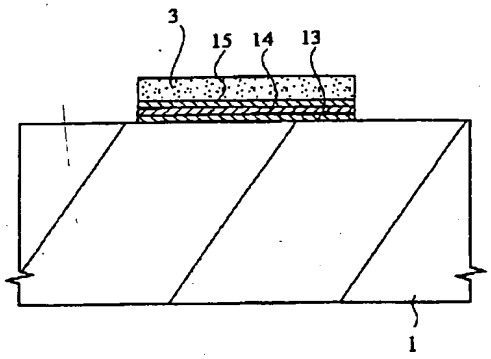

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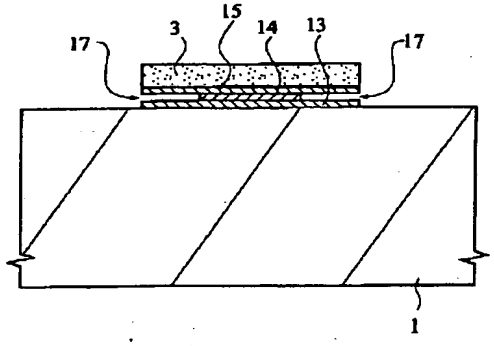
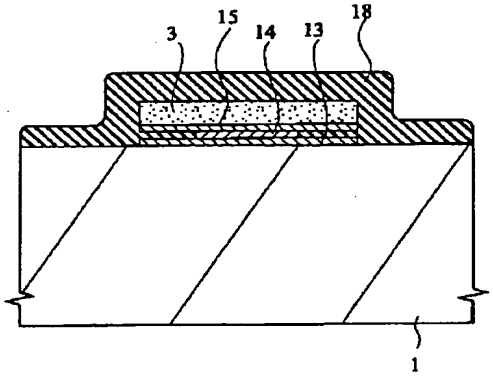
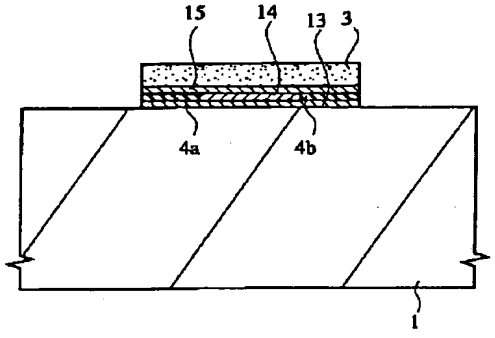


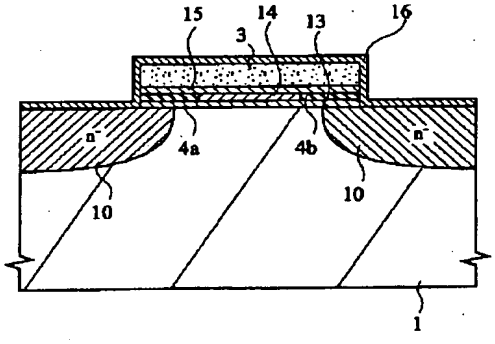
【図１６】



【図１７】



【図１８】



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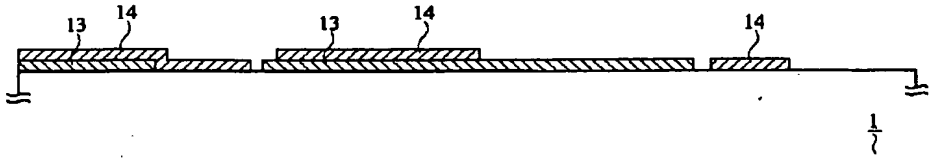

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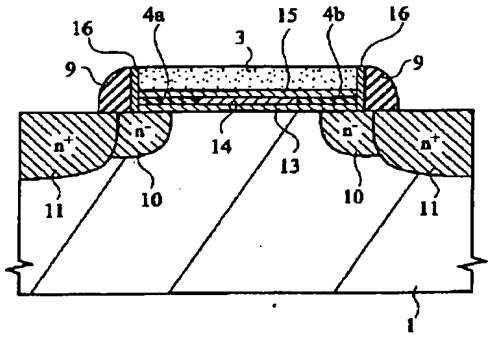

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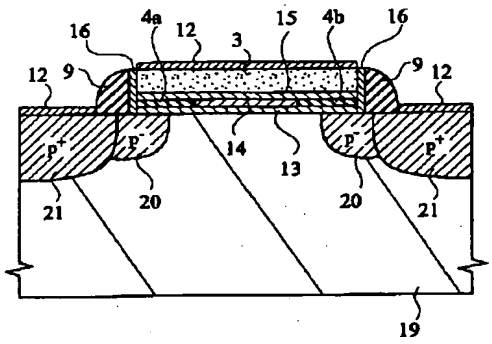

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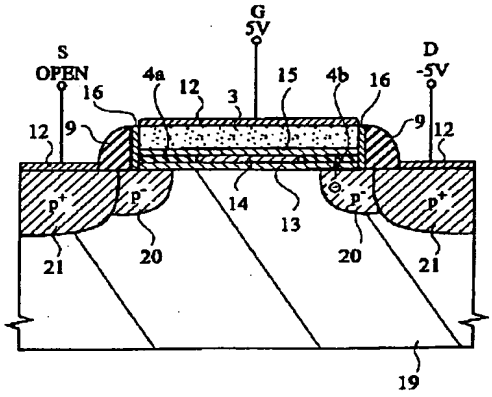

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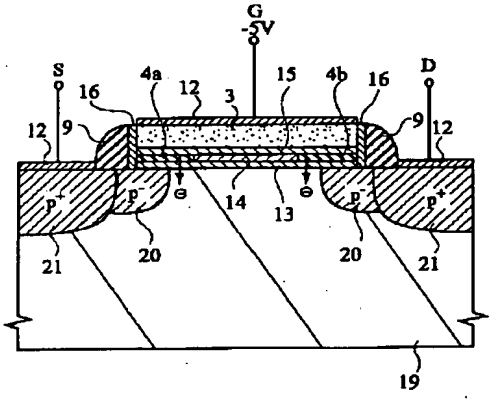
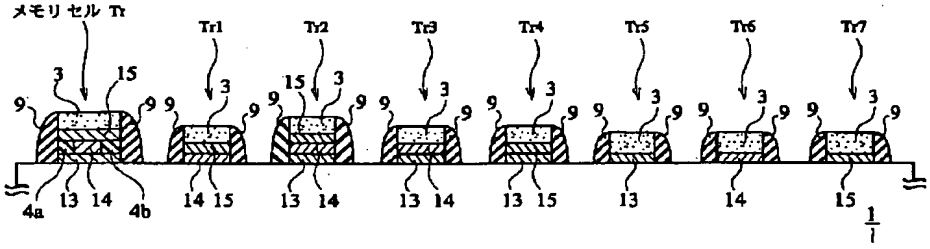


【図２３】



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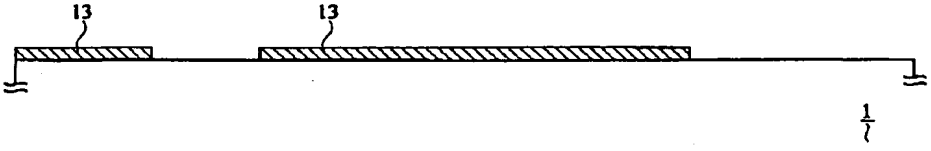

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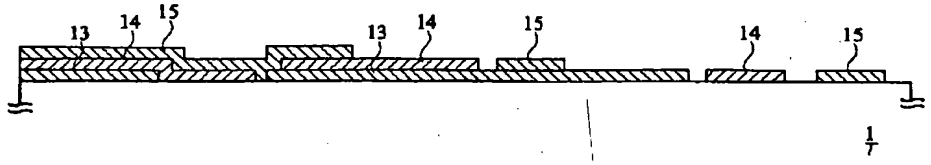

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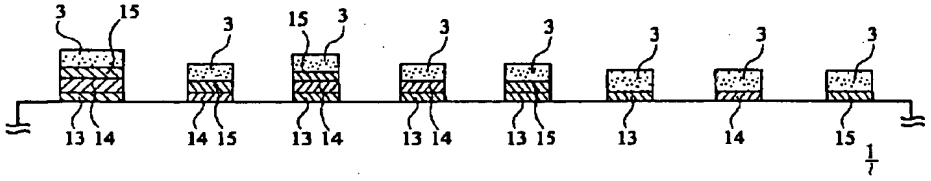

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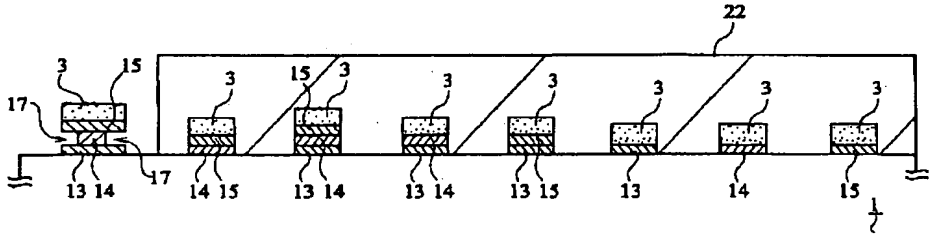

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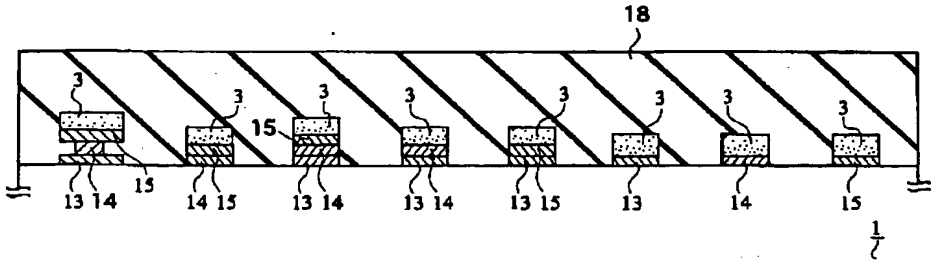

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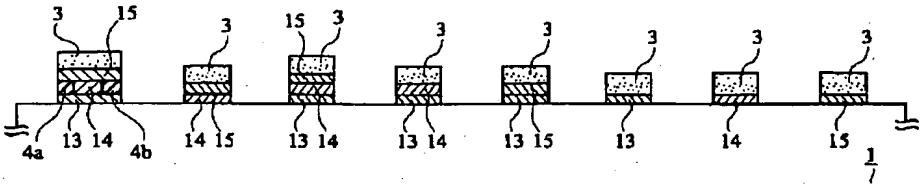

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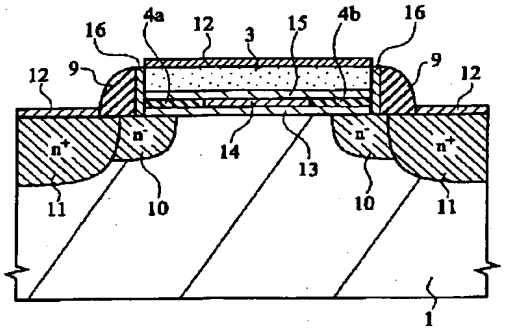

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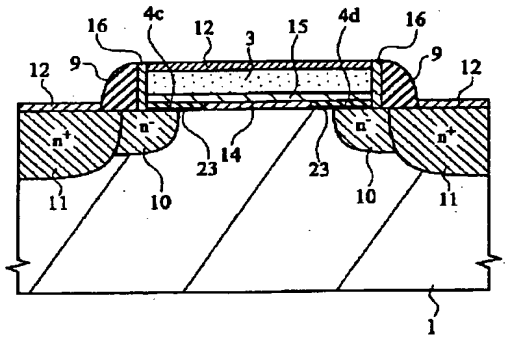

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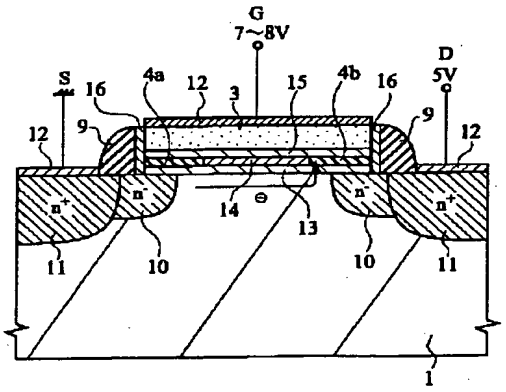

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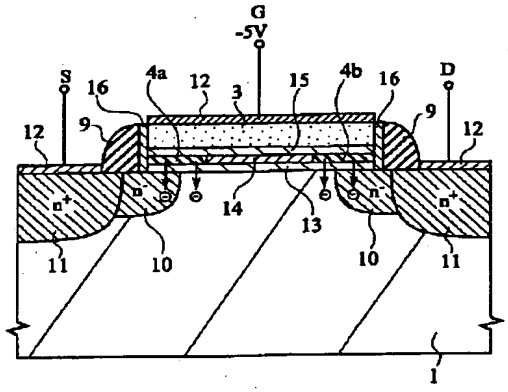

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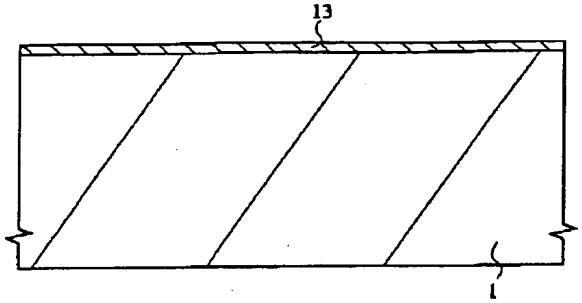

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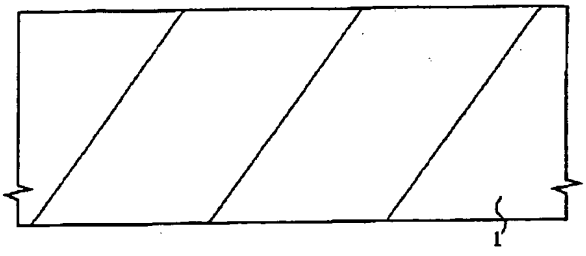

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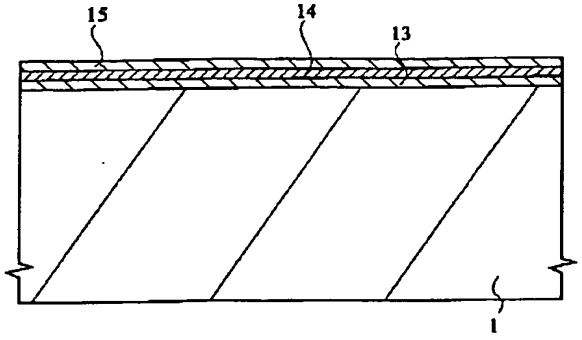

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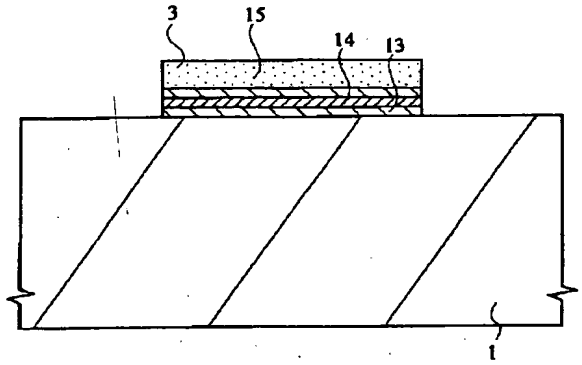

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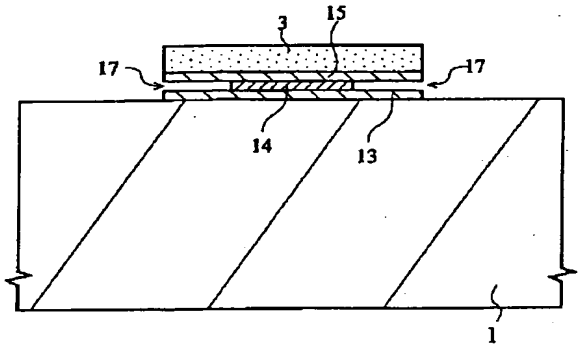

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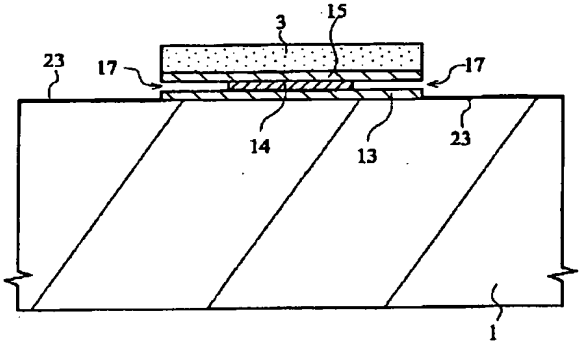

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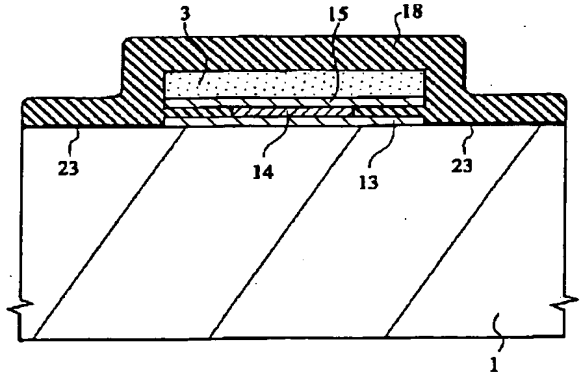

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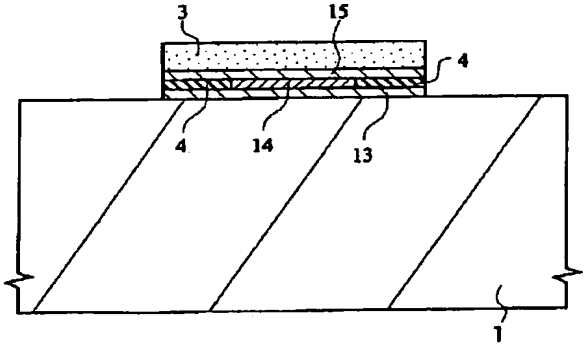

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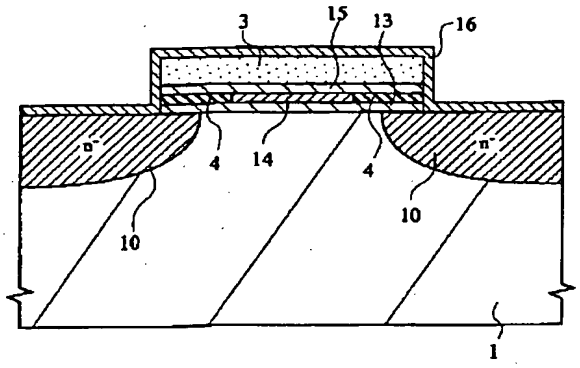

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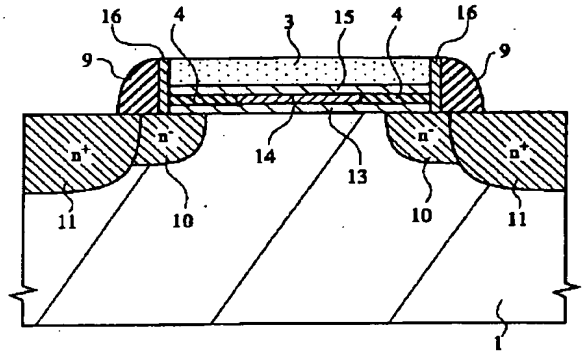

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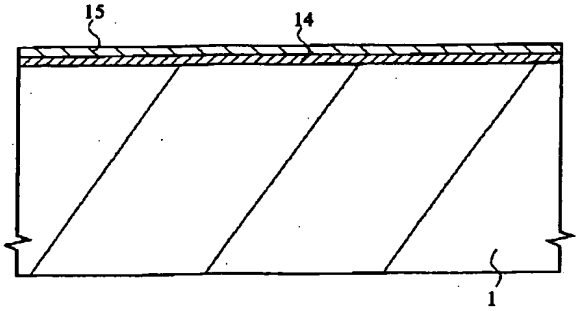

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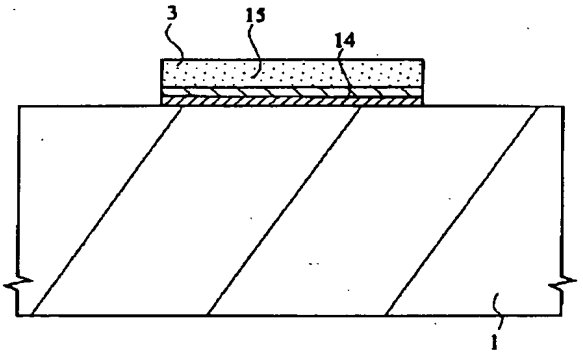

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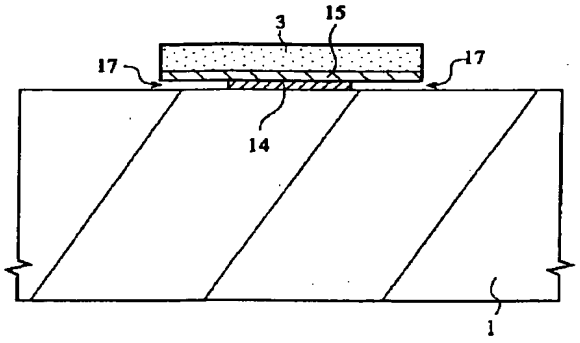

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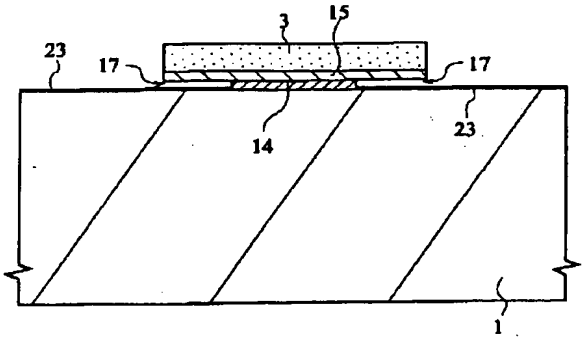

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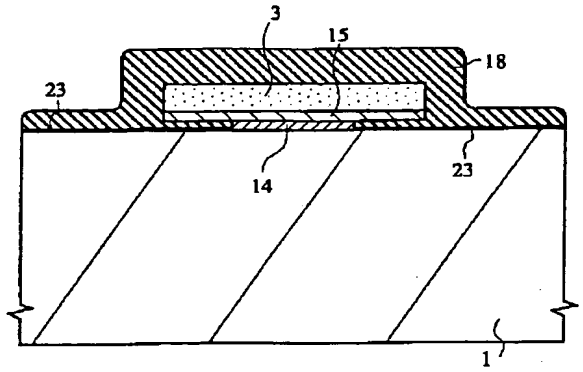

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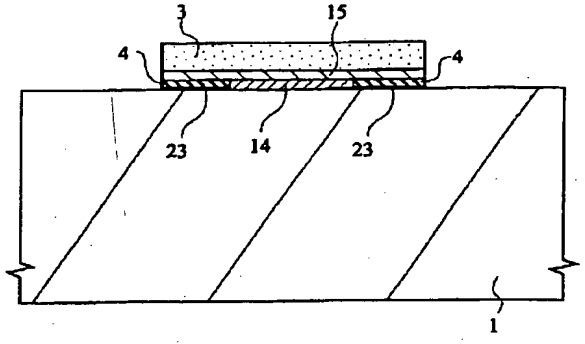

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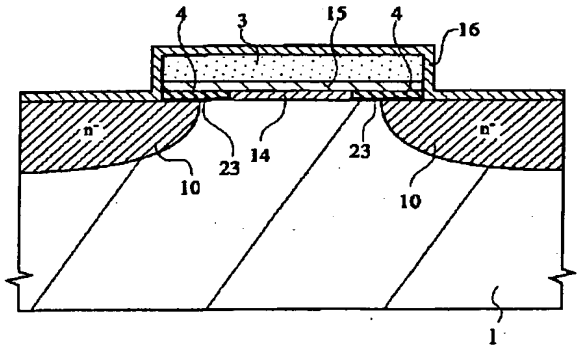

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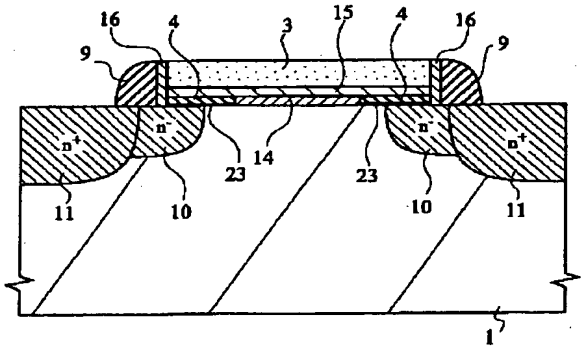

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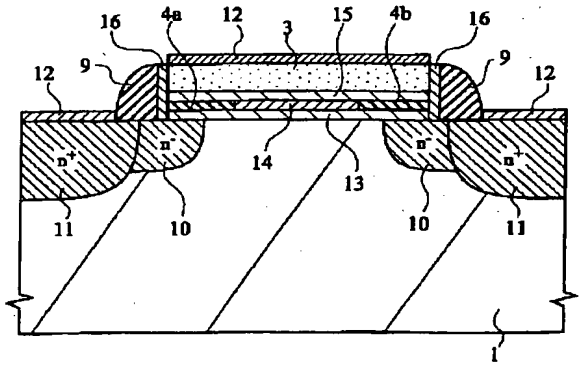

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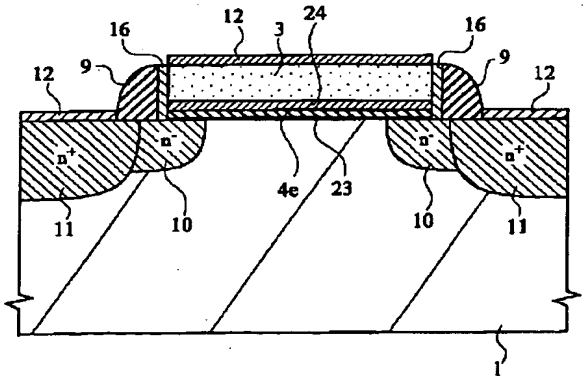

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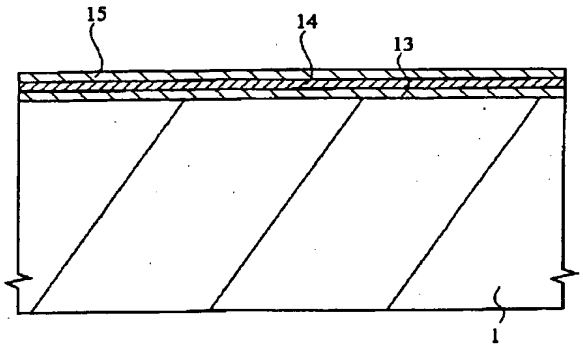

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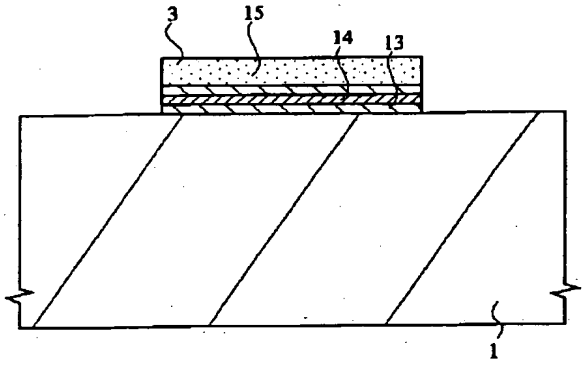

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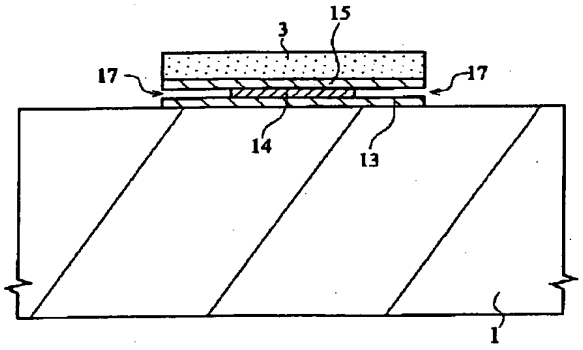

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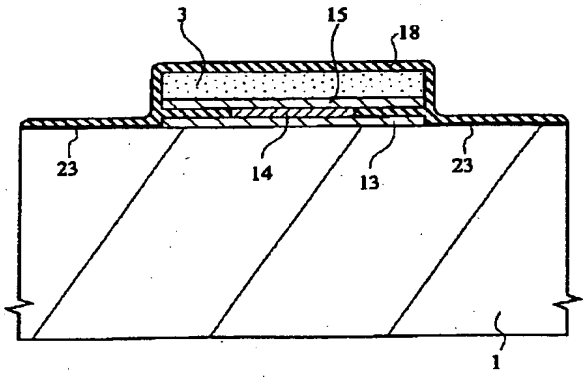

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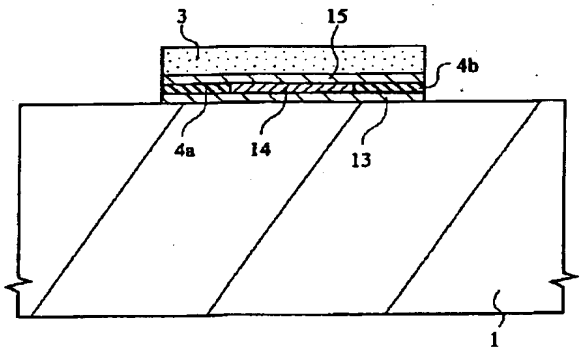

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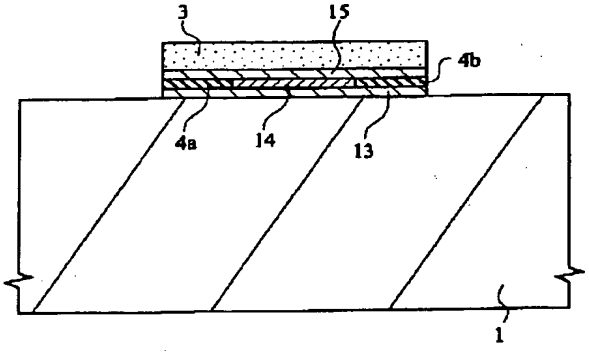

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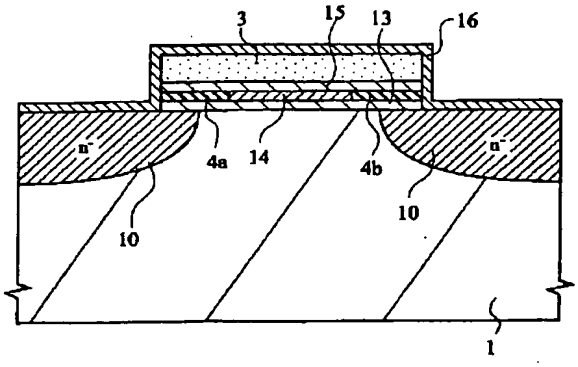

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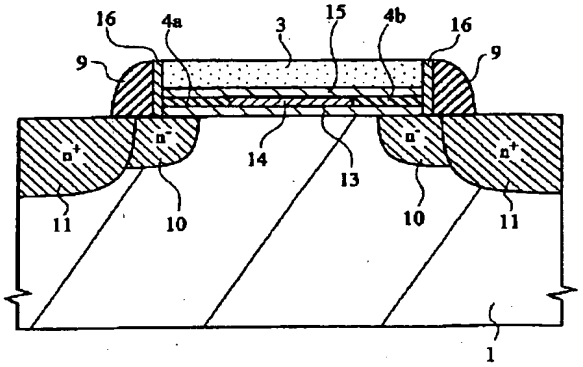

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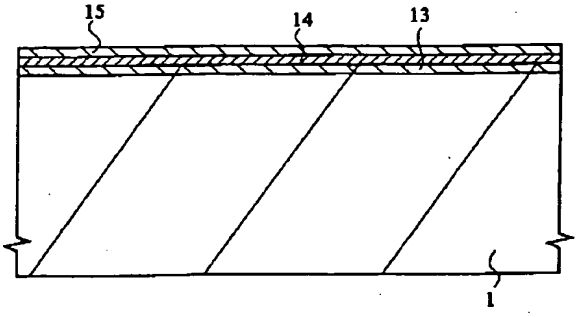

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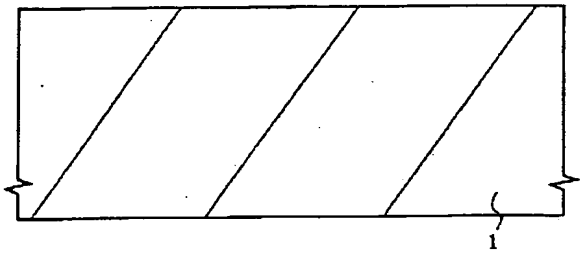

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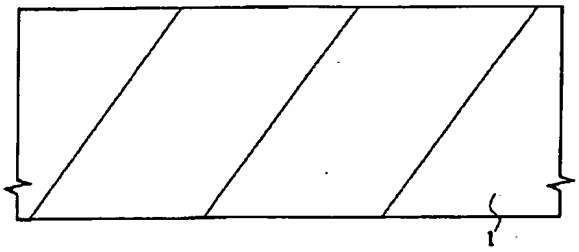

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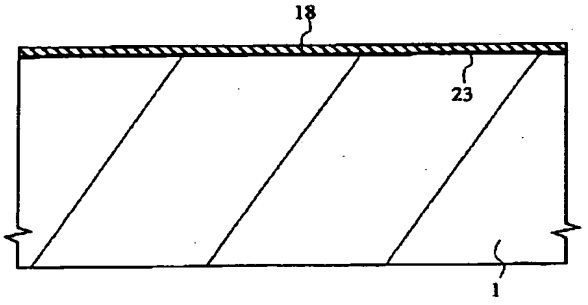

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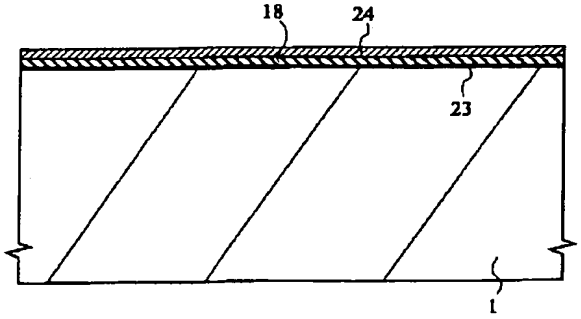

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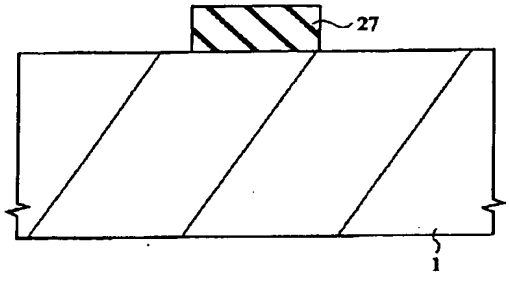

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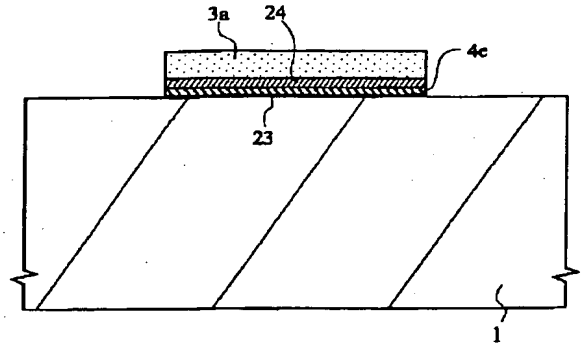

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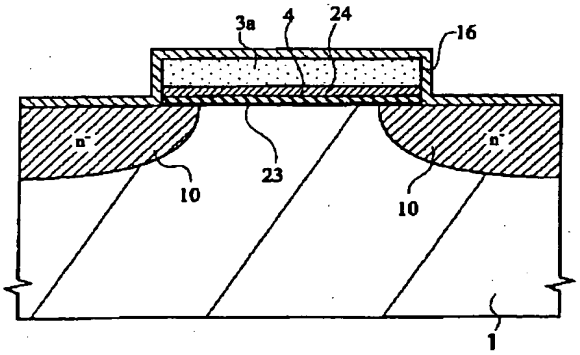

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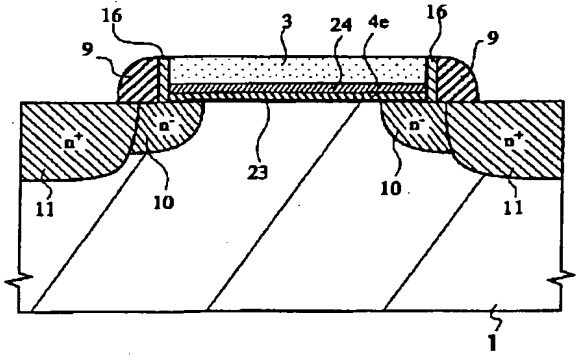

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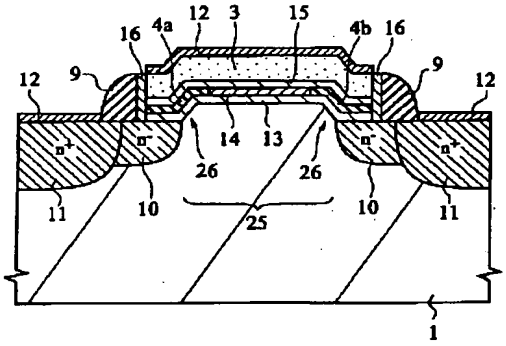

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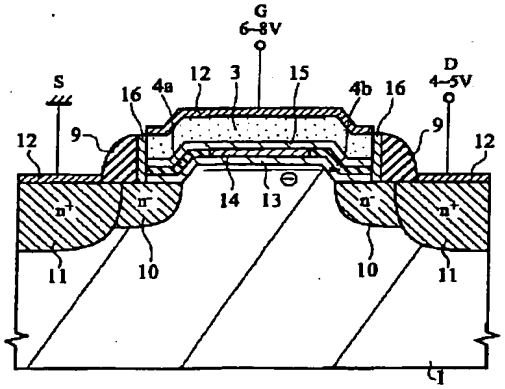

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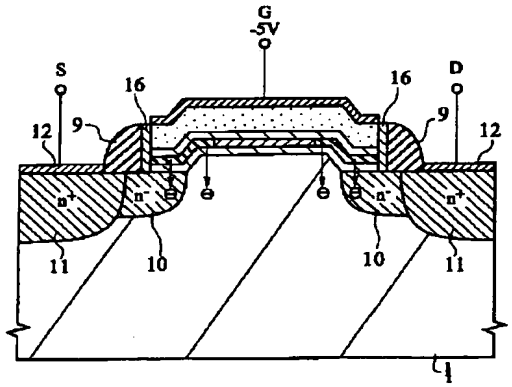

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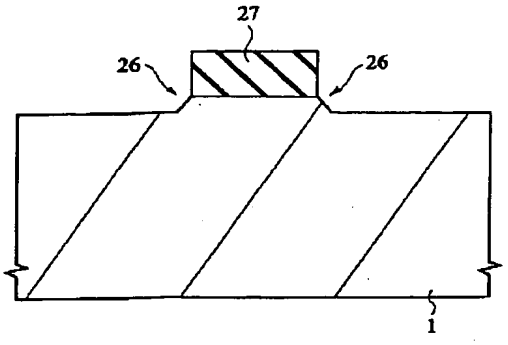

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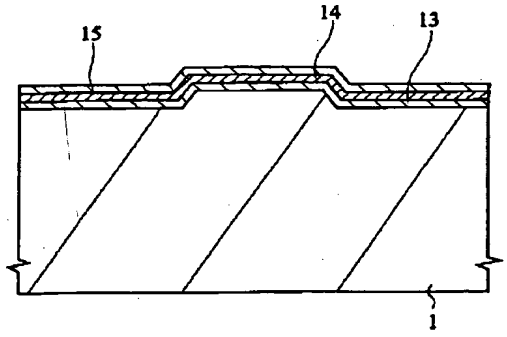

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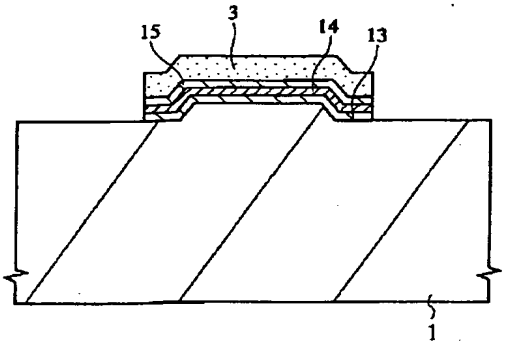

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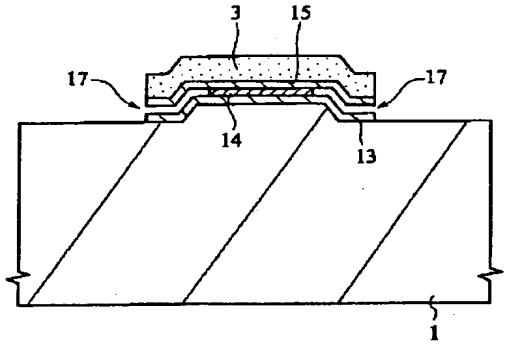

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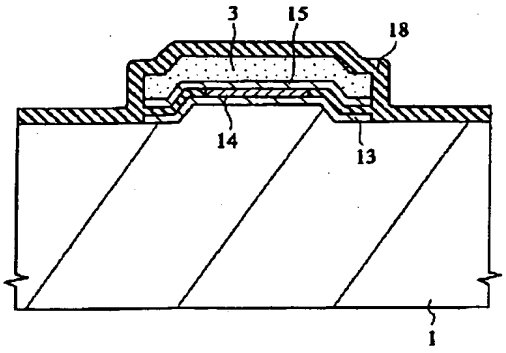

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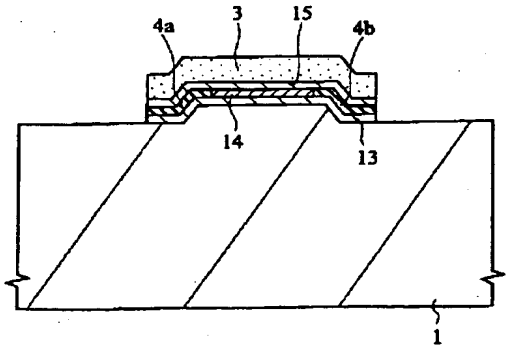

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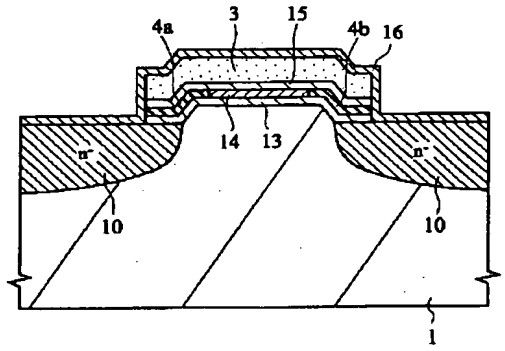

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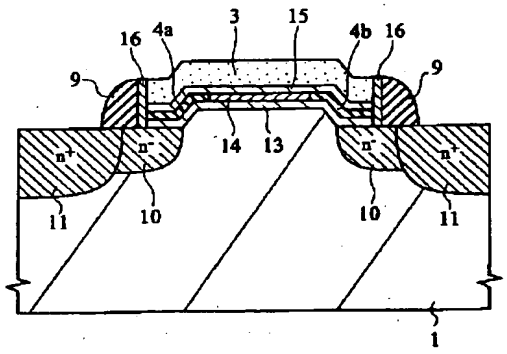

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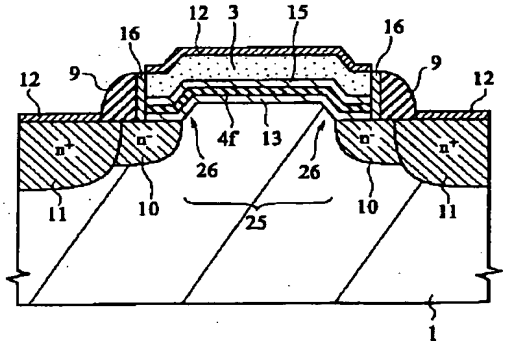

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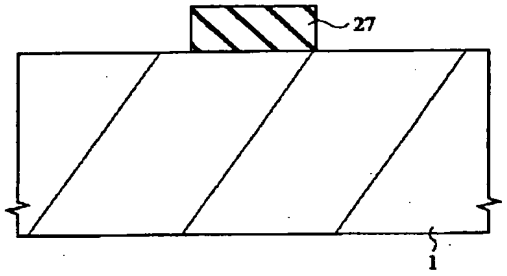

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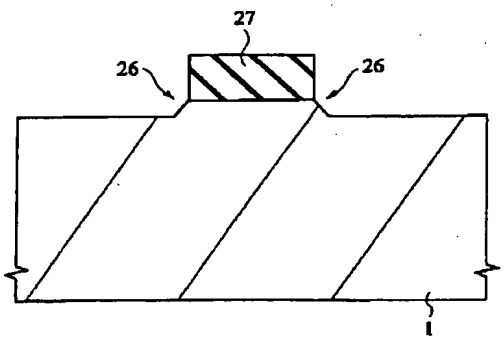

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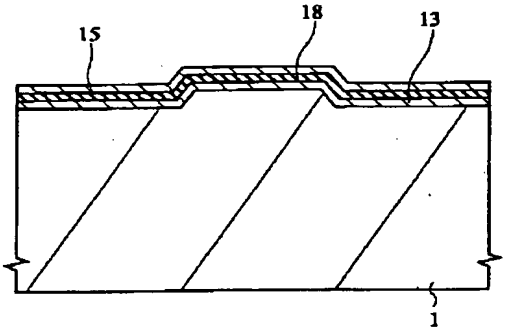

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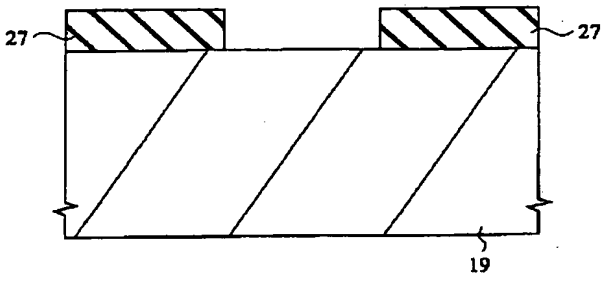

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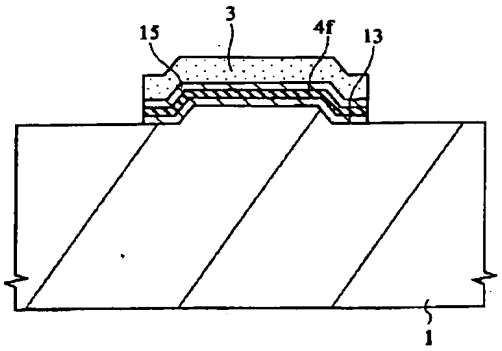

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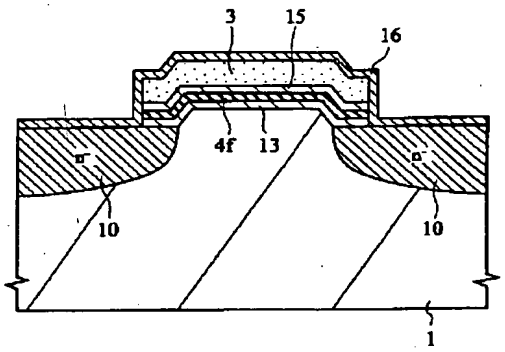

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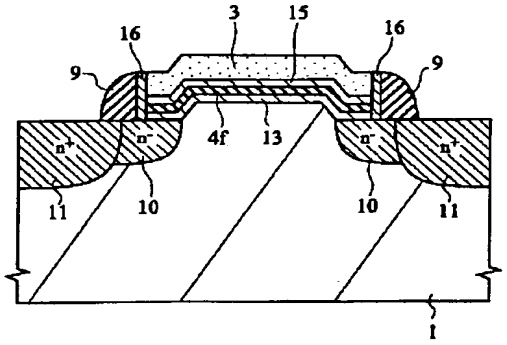

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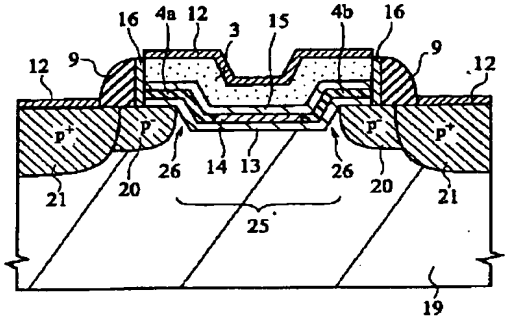

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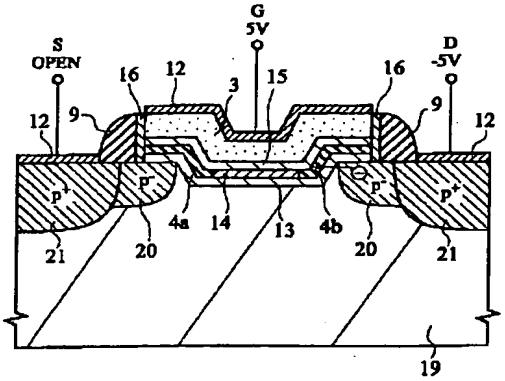

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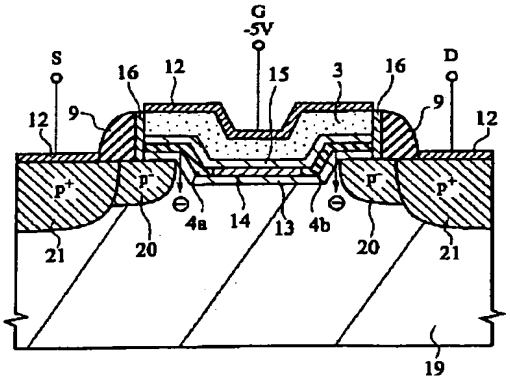

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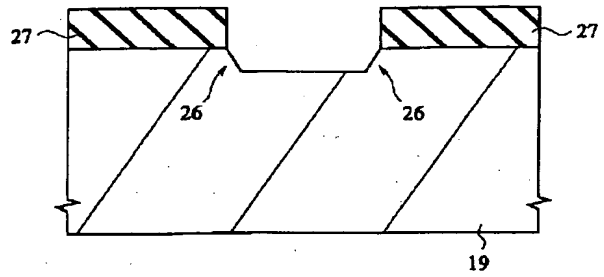

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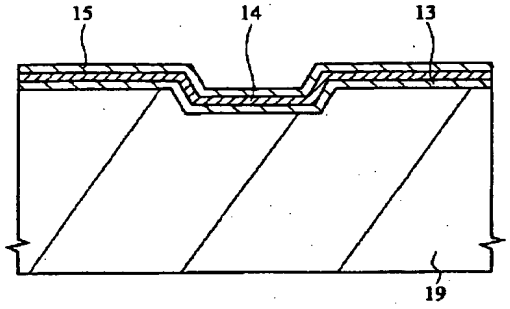

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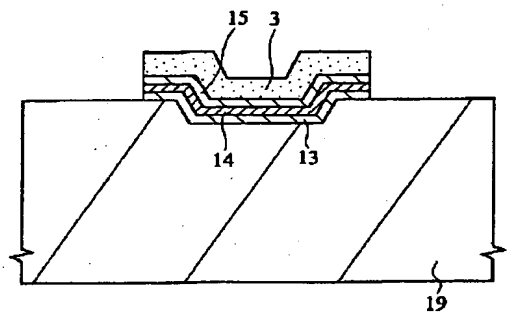

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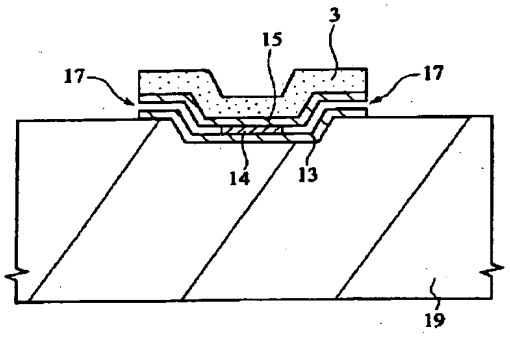

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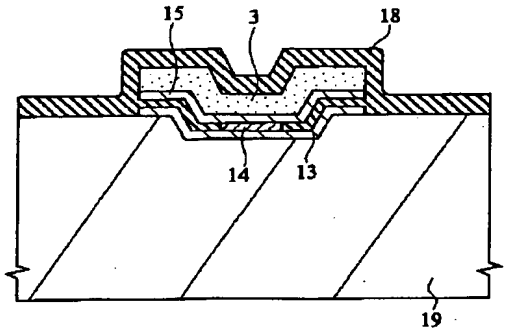

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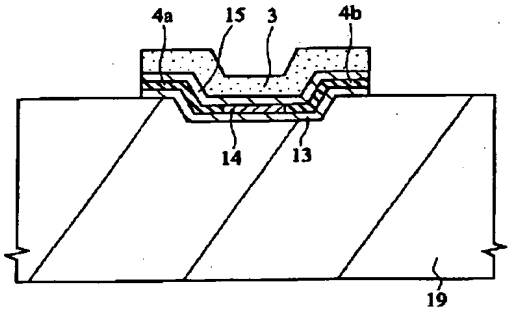

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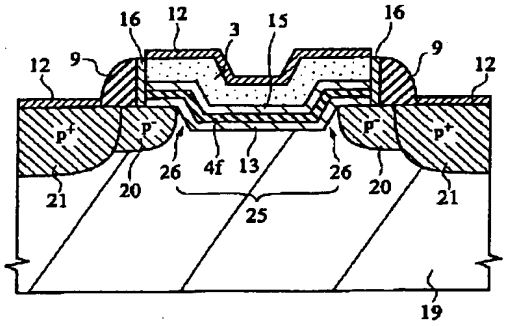

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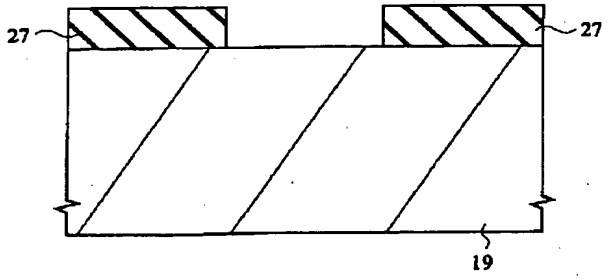

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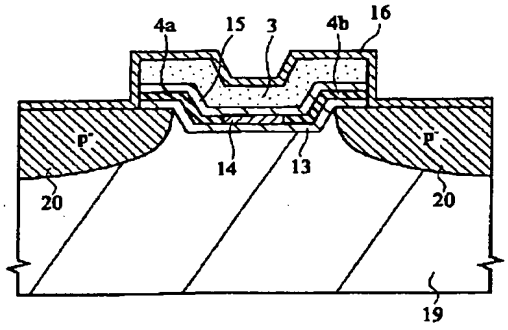

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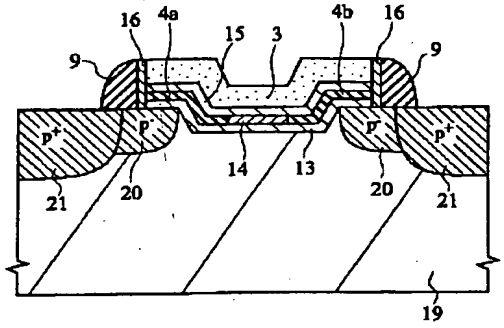

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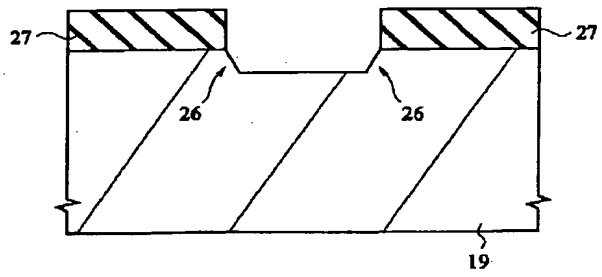

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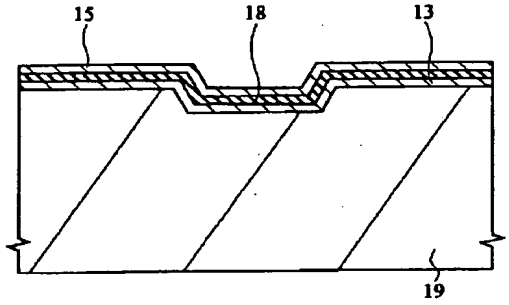

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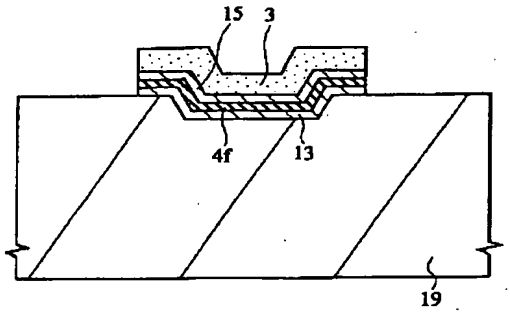

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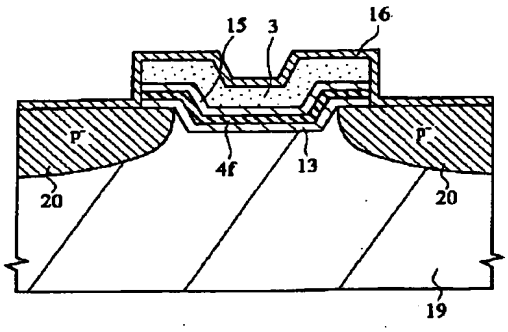

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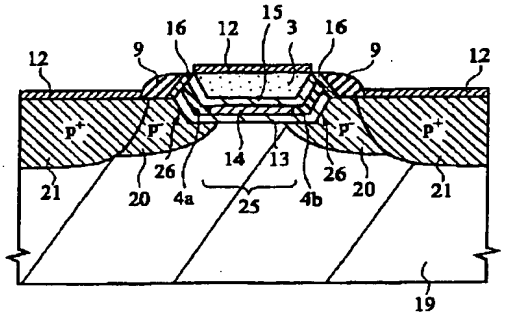

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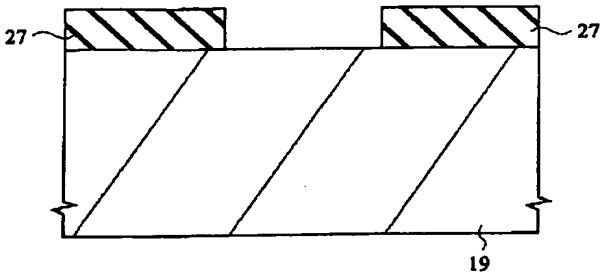

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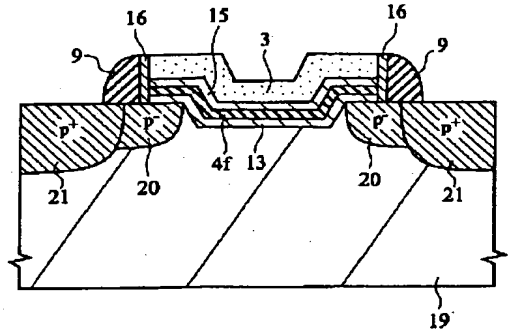

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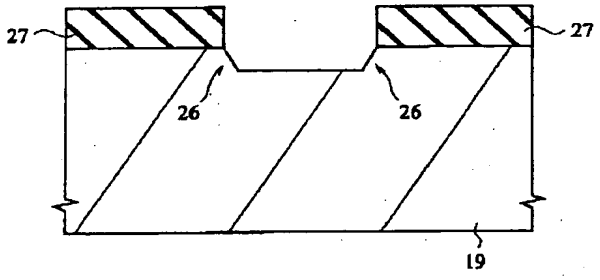

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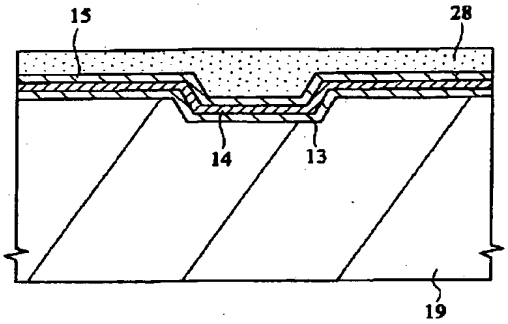

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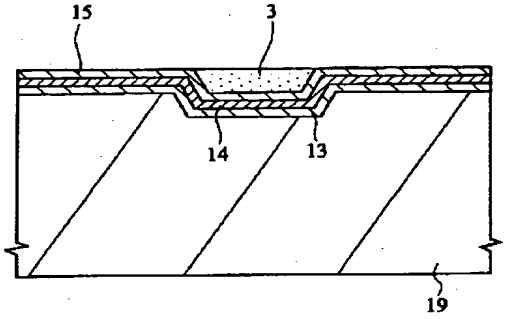

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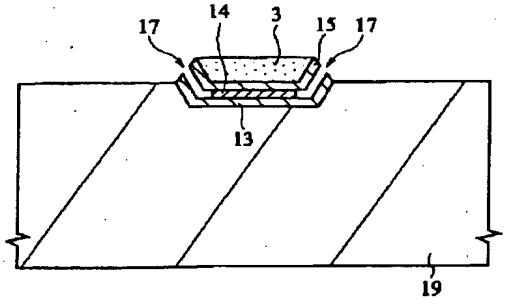

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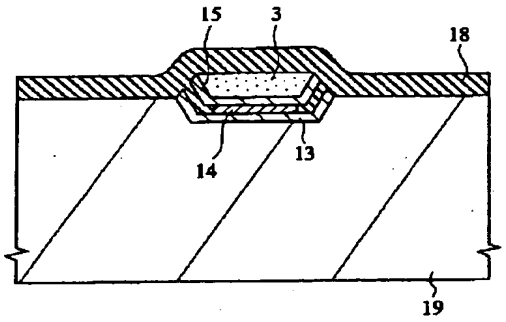

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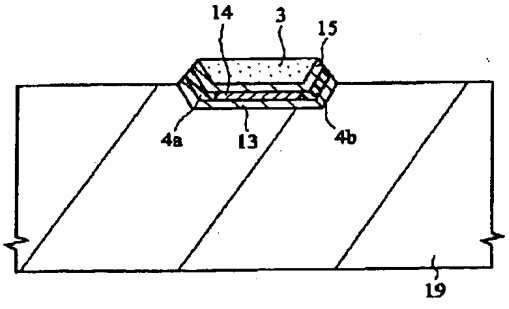

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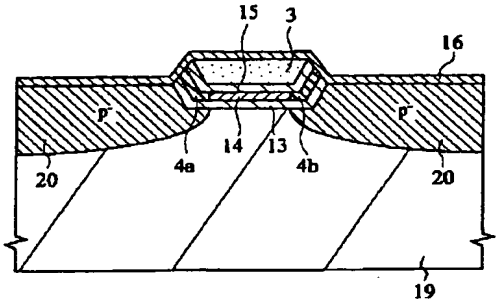

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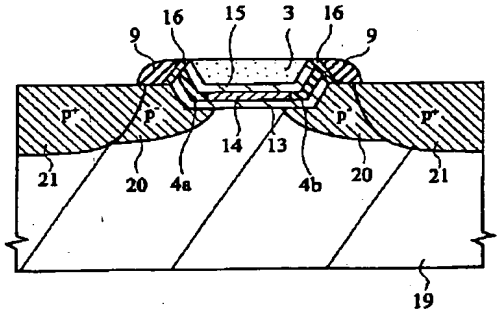

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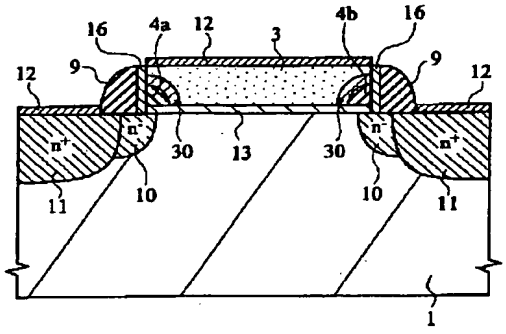

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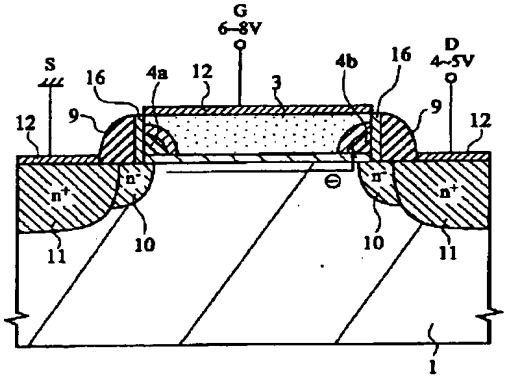

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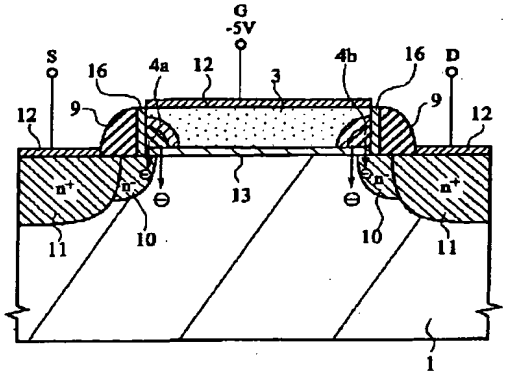

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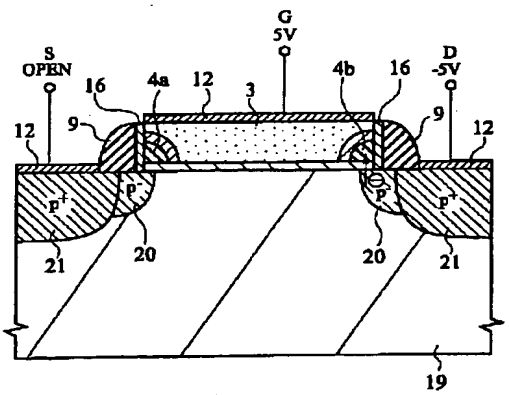

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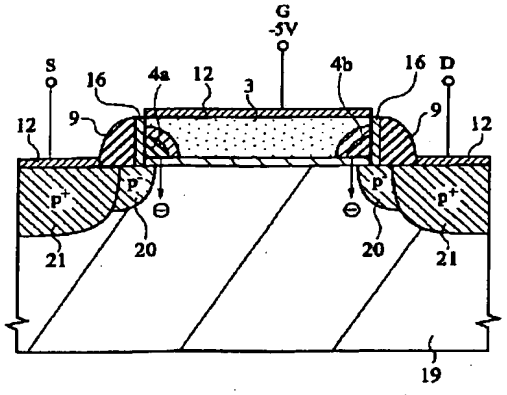

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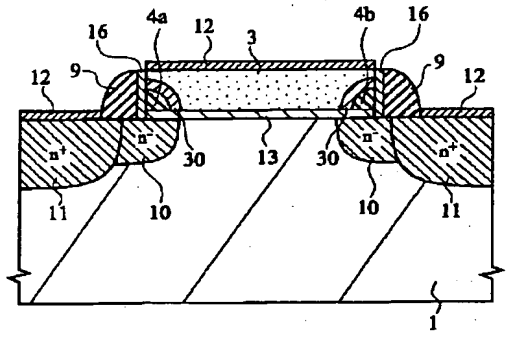

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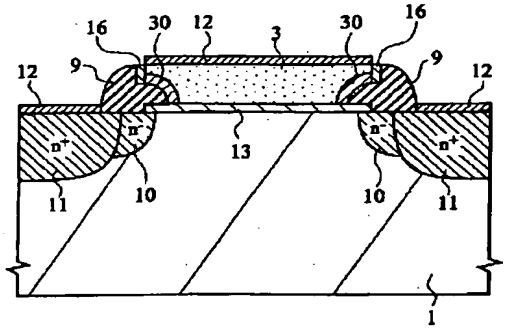

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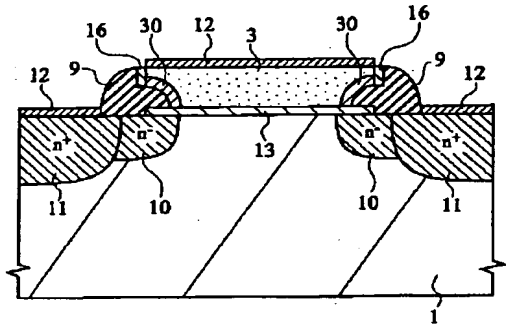

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(54) SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR MANUFACTURING THE SAME

(57) Abstract: PROBLEM TO BE SOLVED: To provide a nonvolatile semiconductor storage device for storing information for plural bits, using a simple cell structure.SOLUTION: In this new structure of a nonvolatile semiconductor storage device for storing information for plural bits, the edge part of a gate electrode is provided with a charge-storing layer 4 for storing electrons. Thus, information on plural bits can be stored by storing the electrons in the charge storage layer 4.

[Claim(s)]
[Claim 1] A nonvolatile semiconductor memory characterized by having
a 1st gate electrode arranged via a gate insulator layer on the principal plane of a semiconductor substrate,
the aforementioned charge accumulation layer arranged on the side face of said 1st gate electrode,
a 2nd gate electrode on the side face of said 1st gate electrode with the charge accumulation layer inbetween, and
an electric conduction layer which connects electrically said 1st and 2nd gate electrodes.

[Claim 2] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms the 1st gate electrode over a gate insulator layer on the principal plane of a semiconductor substrate,
the process which forms a charge accumulation layer and the 2nd gate electrode one by one on the side face of said 1st gate electrode, and
the gate electrode of the above 1st and the gate electrode of the above 2nd.
the process which forms the electric conduction layer which connects electrically

[Claim 3] The nonvolatile semiconductor memory characterized by having
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of a semiconductor substrate,
the charge accumulation layer arranged at the edge of the 2nd aforementioned insulator layer, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 4] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process of forming the 1st, the 2nd, and 3rd insulator layers one by one in this order on the principal plane top of a semiconductor substrate and which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers,
the process which forms a gate electrode by carrying out patterning of this gate electrode component and a gate insulator layer after depositing a gate electrode component on the upper part of this gate insulator layer,
the process which removes the edge of the 2nd aforementioned insulator layer alternatively and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 5] The semiconductor memory characterized by providing
the nonvolatile semiconductor memory which has
the 1st lower insulator layer arranged on the principal plane of a semiconductor substrate,
the 1st middle insulator layer arranged at the upper part of the center of the 1st lower insulator layer,
the 1st charge accumulation layer arranged at the upper part of the edge of the above 1st lower insulator layer,
the 1st upper insulator layer arranged at the upper part of the above 1st middle insulator layer and the 1st charge accumulation layer, and
the 1st gate electrode arranged at the upper part of the 1st up insulator layer
and
the volatile semiconductor memory which has
the 2nd lower insulator layer which has been arranged on the principal plane of the aforementioned semiconductor substrate and which consists of the same material as the interval insulator layer of the above 1st,
the ultra-thin insulator layer arranged on the principal plane top of the aforementioned semiconductor substrate and to the ends of the 2nd lower insulator layer,
the 2nd charge accumulation layer which has been arranged at the upper part of this ultra-thin

insulator layer and which consists of the same material as the above 1st charge accumulation layer,
the 2nd upper insulator layer which has been arranged at the upper part of the above 2nd lower insulator layer and the 2nd charge accumulation layer and which consists of the same material as the above 1st upper insulator layer, and
the 2nd gate electrode arranged at the upper part of the 2nd upper insulator layer.

[Claim 6] the semiconductor memory characterized by providing
the nonvolatile semiconductor memory which has
the 1st lower insulator layer arranged on the principal plane of a semiconductor substrate
the 1st middle insulator layer arranged at the upper part of the center of the 1st lower insulator layer,
the 1st charge accumulation layer arranged at the upper part of the edges of the above 1st lower insulator layer,
the 1st upper insulator layer arranged at the upper part of the above 1st interval insulator layer and the 1st charge accumulation layer, and
the 1st gate electrode arranged at the upper part of the 1st upper insulator layer,
and
the volatile semiconductor memory which has
the ultra-thin insulator layer arranged on the principal plane of the aforementioned semiconductor substrate,
the 2nd charge accumulation layer which has been arranged on this ultra-thin insulator layer and which consists of the same material as the above 1st charge accumulation layer,
the 2nd upper insulator layer arranged on the 2nd charge accumulation layer, and
the 2nd gate electrode arranged on the 2nd upper insulator layer.

[Claim 7] The volatile semiconductor memory characterized by having
the lower insulator layer which has been arranged on the principal plane of a semiconductor substrate,
the ultra-thin insulator layer arranged on top of the principal plane of the aforementioned semiconductor substrate and at the ends of this lower insulator layer,
the charge accumulation layer arranged at the upper part of this ultra-thin insulator layer,
the upper insulator layer arranged on top of the aforementioned lower insulator layer and a charge accumulation layer, and
the gate electrode arranged at the upper part of this up insulator layer .

[Claim 8] The volatile semiconductor memory characterized by having
the ultra-thin insulator layer arranged on the principal plane of a semiconductor substrate,
the charge accumulation layer arranged on this ultra-thin insulator layer,
the insulator layer arranged on this charge accumulation layer, and
the gate electrode arranged on this insulator layer.

[Claim 9] The semiconductor memory characterized by including at least
the process which forms the 1st insulator layer on part of the principal plane of a semiconductor substrate,
the process which forms the 2nd and 3rd insulator layers one by one in the part other than on the principal plane of the aforementioned semiconductor substrate and the upper part of this 1st insulator layer,
the process which deposits a gate electrode component on the upper part of this 3rd insulator layer,
the process which forms the 1st gate electrode by carrying out patterning of this gate electrode component, the 3rd aforementioned insulator layer, the 2nd aforementioned insulator layer and the 1st insulator layer,
the process which forms the 2nd gate electrode by carrying out patterning of the aforementioned gate electrode component, the aforementioned 3rd insulator layer and the 2nd insulator layer,
the manufacture technique process which removes alternatively the edge of the 2nd insulator

layer of both the 1st and 2nd gate electrodes, and thereby forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 10] The manufacture technique of the semiconductor memory characterized by including at least
the process which forms the 1st, the 2nd, and 3rd insulator layers one by one on the principal plane of a semiconductor substrate,
the process which forms the 1st gate electrode by carrying out patterning this gate electrode component, the 3rd aforementioned insulator layer, the 2nd aforementioned insulator layer and the 1st insulator layer after depositing the 1st gate electrode component on the upper part of this 3rd insulator layer,
the process which forms the 2nd gate electrode formation field by removing the aforementioned gate electrode component, the 3rd aforementioned insulator layer, the 2nd aforementioned insulator layer and the 1st insulator layer of part of principal plane of the aforementioned semiconductor substrate, the process being simultaneously process performed with the 1st gate electrode formation process,
the process which removes alternatively the edge of the 2nd insulator layer of the above 1st gate electrode, and forms space,
the process which forms an ultra-thin insulator layer on the principal plane of the aforementioned semiconductor substrate,
the process which forms a charge accumulation layer in the space of the above 1st gate electrode by carrying out anisotropic etching of this charge accumulation layer component after depositing the material which constitutes a charge accumulation layer
the process which forms the 2nd gate electrode by carrying out patterning of the 2nd gate electrode component, the aforementioned 4th insulator layer, aforementioned charge accumulation layer component and ultra-thin insulator layer, after depositing the 4th insulator layer and the 2nd gate electrode component on the principal plane of the aforementioned semiconductor substrate.

[Claim 11] The nonvolatile semiconductor memory characterized by having
the heights arranged on the principal plane of a semiconductor substrate,
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing these heights,
the charge accumulation layer arranged at the edge of the 2nd aforementioned insulator layer, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 12] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a heights on the principal plane of a semiconductor substrate,
the process which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers by forming the 1st, the 2nd, and 3rd insulator layers one by one on the aforementioned semiconductor substrate containing these heights,
the process which forms a gate electrode by carrying out patterning of this gate electrode component and a gate insulator layer after depositing a gate electrode component on the upper part of this gate insulator layer,
the process which removes the edge of the 2nd aforementioned insulator layer alternatively, and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 13] The nonvolatile semiconductor memory characterized by having
the heights arranged on the principal plane of a semiconductor substrate, and
the gate insulator layer which consists of the 1st and 2nd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing this heights,
the charge accumulation layer arranged between the 1st and 2nd insulator layers, and
the gate electrode arranged on the aforementioned gate insulator layer

[Claim 14] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a heights on the principal plane of a semiconductor substrate,
the process that forms the 1st insulator layer, a charge accumulation layer component and the 3rd insulator layer one by one, on the aforementioned semiconductor substrate containing this heights, and
the process which forms a gate electrode by carrying out patterning of this 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer.

[Claim 15] The nonvolatile semiconductor memory characterized by having
the concavity arranged on the principal plane of a semiconductor substrate,
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing this concavity,
the charge accumulation layer arranged at the edge of the aforementioned 2nd insulator layer, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 16] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate,
the process which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers, by forming the 1st, the 2nd, and 3rd insulator layers one by one on the aforementioned semiconductor substrate containing this concavity,
the process which forms a gate electrode by carrying out patterning of this gate electrode component and a gate insulator layer after depositing a gate electrode component on the upper part of this gate insulator layer,
the process which removes the edge of the 2nd aforementioned insulator layer alternatively, and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 17] The nonvolatile semiconductor memory characterized by having
the concavity arranged on the principal plane of a semiconductor substrate,
the gate insulator layer which consists of the 1st and 2nd insulator layers arranged on the principal plane of the aforementioned semiconductor substrate containing this concavity,
the charge accumulation layer arranged between the 1st and 2nd insulator layers, and
the gate electrode arranged on the aforementioned gate insulator layer.

[Claim 18] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate,
the process that forms the 1st insulator layer, a charge accumulation layer component and the 3rd insulator layer, one by one, on the aforementioned semiconductor substrate containing this heights,
the process which forms a gate electrode by carrying out patterning of this 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer.

[Claim 19] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate,
the process which forms the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers by forming the 1st, the 2nd, and 3rd insulator layers one by one on the aforementioned semiconductor substrate containing this concavity,
the process which forms the gate electrode embedded at the aforementioned concavity by removing this gate electrode component by the chemical mechanical polishing technique after depositing a gate electrode component on the upper part of this gate insulator layer,

the process which removes the edge of the aforementioned 2nd insulator layer alternatively, and forms space, and
the process which forms a charge accumulation layer in this space.

[Claim 20] The manufacture technique of the nonvolatile semiconductor memory characterized by including at least
the process which forms a concavity on the principal plane of a semiconductor substrate, and
the process which forms the 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer one by one on the principal plane of the aforementioned semiconductor substrate containing this concavity,
the process which forms the gate electrode embedded at the aforementioned concavity by removing this gate electrode component by the chemical mechanical polishing technique after depositing a gate electrode component on the upper part of this 3rd insulator layer.

[Claim 21] The nonvolatile semiconductor memory characterized by having
the gate electrode arranged through a gate insulator layer on the principal plane of a semiconductor substrate,
the concavity arranged at the edge of this gate electrode, and
the charge accumulation layer arranged through an insulator layer in the upper part of both a channel field and a source drain field at this concavity.

[Detailed Description of the Invention]

[0001] [The technical field to which invention belongs]
This invention relates to an electrically programmable and erasable nonvolatile semiconductor memory and its manufacture technique, a high speed programmable and readable volatile semiconductor memory and its manufacture technique, and a semiconductor memory having a nonvolatile semiconductor memory and a volatile semiconductor memory on the same chip, and its manufacture technique.

[0002] [Description of the Prior Art]
In non-volatile memories, such as conventional EEPROMs (Electrically Erasable and Programmable Read Only Memory), a 1 bit information is memorized in one cell by realizing two different thresholds in one cell.
On the other hand, for the formation of memory high-density, four or more thresholds are given to one cell, and the technique of memorizing the above information in one cell by 2 bits is proposed (M. Bauer et al., ISSCC95, and p.132).
However, in order to realize this technique, an exact control of the threshold voltages, the exact detection for small changes of threshold voltage, and further, a charge hold reliability more than the former are required.
Therefore, with this technique, a performance equivalent to the former can actually not necessarily be obtained.
Moreover, this technique also has the problem, that the manufacture yield is low.
For this reason, the cellular structure which memorizes a plurality of bit information by accumulating a charge in a plurality of physically different positions is newly proposed (B. Eitan et al, IEDM96, p169, and Fig. 6).
Moreover, as a similar cellular structure to this, a structure providing a charge accumulation layer on the side wall of the gate electrode has been proposed by this invention person before (U.S. patent number of No. 4881108).
However, the manufacturing process of these cellular structures is very complicated, and has the problem that the controllability of a channel field is not enough, either.

[0003] On the other hand, from the demand for system-on-chips of these days, the necessity of realizing an electrically writing-in erasable non-volatile memory and a high speed writing-in read-out erasable volatile memory on the same chip is increasing.
Especially, the demand for VLSI, which combine a high speed operation dynamic RAM and a non-volatile memory with a floating-gate structure such as EEPROM and flash memory, is increasing rapidly.
However, the memory cell of a dynamic RAM in recent years has very complicated three-dimensional structure called trench structure and stack structure.
For this reason, if it is going to combine floating-gate type non-volatile memory and a dynamic RAM, from the difference in the memory cell structure, a manufacture process will be complicated and the number of mask processes will also increase.
Therefore, the manufacturing cost of the combined chip will become very big.

[0004] If the memory cell of a dynamic RAM is realized using the memory cell structure of non-volatilized floating-gate type memory, it is possible for a manufacture process to be simplified by communalization of the cellular structure and to reduce a manufacturing cost by it.
However, in the communalized memory cell, it is difficult to realize the high-speed writing which is the characteristic feature of a dynamic RAM.

[0005] [Problem(s) to be Solved by the Invention]
This invention is accomplished in view of the above-mentioned situation, and aims at offering the structure of the nonvolatile semiconductor memory which can memorize the two or more bit information with an easy cellular structure.

[0006] Other purposes of this invention are offering the manufacture technique of the nonvolatile

semiconductor memory which manufactures the nonvolatile semiconductor memory which memorizes a two or more bit information in an easy manufacture process.

[0007] The further other purpose of this invention is offering the structure of a semiconductor memory with an easy cellular structure having an electrically programmable erasable non-volatile memory and a high-speed read-out write-in volatile memory combined.

[0008] The further other purpose of this invention is offering the manufacture technique of a semiconductor memory with an easy manufacture process having an electrically programmable erasable non-volatile memory and a high-speed read-out write-in volatile memory combined.

[0009] [Means for Solving the Problem]
In order to attain the above-mentioned purpose, the 1st characteristic feature of this invention is a nonvolatile semiconductor memory comprising at least
a 1st gate electrode arranged on the principal plane of a semiconductor substrate with a gate insulator layer in-between the two,
a charge accumulation layer on the side face of the 1st gate electrode,
a 2nd gate electrode on the 1st gate electrode with the charge accumulation layer in-between the two,
an electric conduction layer electrically connecting the 1st gate electrode and the 2nd gate electrode.

[0010] The 2nd characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least
the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of a semiconductor substrate,
the charge accumulation layer arranged at the edge of the 2nd insulator layer, and
the gate electrode arranged on the gate insulator layer.

[0011] The 3rd characteristic feature of this invention is a semiconductor memory combining a nonvolatile semiconductor memory and a volatile semiconductor memory,
the nonvolatile semiconductor memory comprising at least
a 1st lower insulator layer arranged on the principal plane of the semiconductor substrate, and
a 1st interval insulator layer arranged at the upper part of the center of the 1st lower insulator layer,
the 1st up insulator layer arranged at the upper part of the 1st charge accumulation layer arranged at the upper part of the edge of the 1st lower insulator layer, and
the 1st interval insulator layer and the 1st charge accumulation layer,
the 1st gate electrode arranged at the upper part of the 1st up insulator layer,
the volatile semiconductor memory comprising at least
a 2nd lower insulator layer which has been arranged on the principal plane of the semiconductor substrate and which consists of the same material as the 1st interval insulator layer,
on the principal plane of a semiconductor substrate, and
the ultra-thin insulator layer arranged to the ends of the 2nd lower insulator layer,
the 2nd charge accumulation layer which has been arranged at the upper part of an ultra-thin insulator layer and which consists of the same material as the 1st charge accumulation layer,
the 2nd gate electrode arranged at the upper part of the 2nd up insulator layer which has been arranged at the upper part of the 2nd lower insulator layer and the 2nd charge accumulation layer, and which consists of the same material as the 1st up insulator layer, and the 2nd up insulator layer.

[0012] The 4th characteristic feature of this invention is a semiconductor memory which combines a nonvolatile semiconductor memory and an volatile semiconductor memory, the nonvolatile semiconductor memory comprising at least the 1st lower insulator layer arranged on the principal plane of a semiconductor substrate, and the 1st interval insulator layer arranged at the upper part of the center of the 1st lower insulator layer, the 1st up insulator layer arranged at

the upper part of the 1st charge accumulation layer arranged at the upper part of the edge of the 1st lower insulator layer, and the 1st interval insulator layer and the 1st charge accumulation layer, the 1st gate electrode arranged at the upper part of the 1st up insulator layer, an volatile semiconductor memory comprising at least the 2nd charge accumulation layer which has been arranged on the ultra-thin insulator layer arranged on the principal plane of a semiconductor substrate, and an ultra-thin insulator layer and which consists of the same material as the 1st charge accumulation layer, the 2nd gate electrode arranged on the 2nd up insulator layer arranged on the 2nd charge accumulation layer and the 2nd up insulator layer.

[0013] The 5th characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least the gate insulator layer which consists of the 1st, the 2nd, and 3rd insulator layers arranged on the principal plane of the semiconductor substrate containing the heights or concavity arranged on the principal plane of a semiconductor substrate, and a heights or a concavity, the charge accumulation layer arranged at the edge of the 2nd insulator layer, and a gate electrode arranged on the gate insulator layer.

[0014] The 6th characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least the charge accumulation layer arranged between the gate insulator layer which consists of the 1st and 2nd insulator layers arranged on the principal plane of the semiconductor substrate containing the heights or concavity arranged on the principal plane of a semiconductor substrate, and a heights or a concavity, and the 1st and 2nd insulator layers, and the gate electrode arranged on a gate insulator layer.

[0015] The 7th characteristic feature of this invention is the nonvolatile semiconductor memory comprising at least the gate electrode arranged on the principal plane of a semiconductor substrate with a gate insulator layer inbetween, the concavity arranged at the edge of a gate electrode, the charge accumulation layer arranged at the concavity with an insulator layer inbetween, and a charge accumulation layer arranged at the upper part of both a channel field and a source drain field.

[0016] [Embodiments of the Invention]
With reference to a drawing, the embodiment forms of this invention are explained below.
In the publication of the following drawings, the same or similar sign is given to the same or similar fraction.
However, a drawing is typical and the proportion of the relation between thickness and a flat-surface dimension and the thickness of each class etc. should regard differing from an actual thing.
Therefore, in consideration of the following explanations, you should judge concrete thickness and a concrete dimension.
Moreover, of course, between drawings the fraction from which the relation and proportion of a mutual dimension, also contain differences.

[0017] (1st Embodiment Form) Fig. 1 is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.
This memory cell consists of an n type MOS transistor.
With the memory cell structure of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention, the 1st gate electrode 3 is formed in the front face of the p type semiconductor substrate 1 through the gate insulator layer 2, and the charge accumulation layer 4 (4a, 4b) is formed on both sides of the 1st gate electrode 3.
This charge accumulation layer 4 has the laminated structure, the 1st layer is oxide film 5, the 2nd layer consist of a nitride 6, and the 3rd layer consists of the 2nd oxide film 7.
Furthermore, the 2nd gate electrode 8 is formed in the upper part of the charge accumulation layer 4.
The side wall spacer 9 is formed in the side face of the charge accumulation layer 4,
and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n-

type diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each front face of the 1st gate electrode 3, the charge accumulation layer 4, the 2nd gate electrode 8, and n+ type diffusion layer 11.
The 1st gate electrode 3 and the 2nd gate electrode 8 are electrically connected through this electric conduction layer 12.

[0018] The memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention has LDD (Lightly Doped Drain) structure which constituted the source field and the drain field, from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration.
And then, the charge accumulation layer 4 is formed in the both sides of 1st gate electrode 3, and the threshold change of potential, which is produced according to the existence of the electron held at the nitride layer 6 of these two charge accumulation layers 4, this threshold change of potential is made to correspond to a storage information "00", "01", "10", and "11".
Furthermore, the 2nd gate electrode 8 is formed in the upper part of the charge accumulation layer 4, by electrically connecting this 2nd gate electrode 8 to the 1st gate electrode 3, the controllability of a channel field is raised and detection for threshold voltage change is made easy.

[0019] Next, an operation of the non-volatile memory concerning the 1st embodiment form of this invention is explained using Fig. 2 to Fig. 4 .
Fig. 2 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 3 is a cross section of the non-volatile memory explaining a read-out operation.
Fig. 4 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 2 , at the time of the writing of a memory cell, the high voltage (-10V) is impressed to gate G, and simultaneously, the high voltage (-8V) is applied to drain D in the proximity of charge accumulation layer 4b which accumulates an electron, and the non-proximity source S is grounded.
Thus, if a voltage is impressed, a channel thermoelectron (Channel Hot Electron) will occur and this thermoelectron will be captured by the nitride 6 of charge accumulation layer 4b.
When the charge accumulation layer 4b captures an electron, the threshold voltage of a cell transistor changes.
Read-out of a memory cell is performed by detecting a part for a threshold change of potential.
Specifically, as shown in Fig. 3 , voltage 5V are added to gate G, voltage 3V are simultaneously impressed to drain D, and the difference of the amount of currents is detected with a sense amplifier.
Moreover, as shown in Fig. 4 , a deletion of a memory cell is performed by impressing a negative voltage (at least - 6V) to gate G, a right voltage (9V) to drain D in the proximity of charge accumulation layer 4b to be erased, and by emitting trapped electron of charge accumulation layer 4b.
In addition, as everyone knows, source S and drain D of an MOS transistor are made symmetrically, and, generally source S and drain D can be changed.
Therefore, also in the above-mentioned explanation, it is possible to replace source S and drain D.

[0020] Next, the manufacture technique of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention is explained using Fig. 5 through Fig. 9 .
As first shown in Fig. 5 , the 25nm gate insulator layer 2 is formed by thermal oxidation on the p type semiconductor substrate 1.
Then, after depositing the 300nm polycrystal silicon layer which is doped by n type or p type impurity by the LPCVD (Low Pressure Chemical Vapor Deposition) method all over p type semiconductor substrate 1, patterning is carried out with well-known exposure technique and well-known etching technique, and the 1st gate electrode 3 is formed.

[0021] Next, as shown in Fig. 6 , after removing the gate insulator layer 2 of the front face of the p type semiconductor substrate 1 of the field which forms a source field and a drain field, the p type semiconductor substrate 1 is oxidized thermally in a 900 degrees C - 1200 degrees C oxidizing atmosphere, and the 1st 10nm oxide film 5 is formed.
And the 10nm - 100nm nitride 6 is deposited by the LPCVD method on the 1st oxide film 5, and after that, the 2nd about 5nm oxide film 7 is formed in nitride 6 front face by 900-degree C hydrogen-burning oxidization or CVD.

[0022] Next, as shown in Fig. 7 , after depositing about 25-250nm polycrystal silicon on the 2nd oxide film 7 by the LPCVD method for example, anisotropic etching by the RIE (Reactive Ion Etching) method is performed, and by removing of this polycrystal silicon layer, the 1st oxide film 5, the nitride 6, and the 2nd oxide film 7 only their film thickness part, the charge accumulation layer 4 which has the 2nd gate electrode 8 in the upper part is formed at the 1st gate electrode side face.

[0023] Next, as shown in Fig. 8 , n- type diffusion layer 10 of low impurity concentration is formed.
It is formed by ion-implantation technique, that is by pouring in n type impurity using the 1st gate electrode 3 and the charge accumulation layer 4 as the mask, and by activating the impurity which was poured in by subsequent heat treatment.

[0024] Next, as shown in Fig. 9 , after forming the side wall spacer 9 in the side wall of the charge accumulation layer 4, n+ type diffusion layer 11 of high impurity concentration is formed.
It is formed by ion-implantation technique, that is by pouring in n type impurity using the 1st gate electrode 3, the charge accumulation layer 4 and the side wall spacer 9 as the mask, and by activating the impurity which was poured in by subsequent heat treatment.

[0025] Next, high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, and then, by heat-treating the p type semiconductor substrate 1 in an inert atmosphere in each front face of the 1st gate electrode 3, the charge accumulation layer 4, the 2nd gate electrode 8, and n+ type diffusion layer 11, the electric conduction layer 12 which consists of a refractory-metal silicide is formed.
At this time, the thickness of the 1st oxide film 5, the nitride 6, the 2nd oxide film 7, especially the nitride 6 needs to be set up so that it may reach 1st gate electrode 3 and the refractory-metal silicide layer on the 2nd gate electrode 8 may carry out a bridging. After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 1 will be completed.

[0026] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 1 , and a final nonvolatile memory cell is completed.

[0027] According to the 1st embodiment form of this invention, since the 2nd gate electrode 8 was formed also in the upper part of the charge accumulation layer 4, the controllability of a threshold voltage improves.
In addition, the same effect is acquired, even if it is the case where it constitutes from a p type MOS transistor, although the 1st embodiment form of this invention explained the case where a memory cell was constituted from an n type MOS transistor.
Moreover, the memory cell has an LDD structure and it may be single drain structure or double drain structure.

[0028] (2nd embodiment form)
Next, the 2nd embodiment form of this invention is explained.

Fig. 10 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.
This memory cell consists of an n type MOS transistor.
With the memory cell structure of the non-volatile memory concerning the 2nd embodiment form of this invention, the 2nd gate insulator layer 14 is formed in the front face of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
And the charge accumulation layers 4a and 4b are formed at the ends of the 2nd gate insulator layer 14.
On the 2nd gate insulator layer 14 and charge accumulation layers 4a and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed on each surface of gate electrode 3 and n+ type diffusion layer 11.

[0029] The memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention has LDD structure which constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration.
And a gate insulator layer consists of three layer cascade screen consisting of 1st gate insulator layer 13 (lower layer), 2nd gate insulator layer 14 (interlayer), and of the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated to these two charge accumulation layers 4a and 4b, the store status being one of the four following status, namely

(1) the status that neither accumulation layer 4a nor 4b are accumulating electrons,
(2) the status that only charge accumulation layer 4a is accumulating the electron,
(3) the status that only charge accumulation layer 4b is accumulating the electron,
(4) the status that charge accumulation layers 4a and 4b are both accumulating the electron.

The amount of threshold change of potential according to the existence/non-existence of the electron held at these two charge accumulation layers 4a and 4b is made to correspond to storage information "00", "01", "10" and "11."
Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located in the upper part of a channel field edge, the threshold voltage of a channel field center section is decided only by impurity concentration of a channel field, and it does not depend for it on the store status of the electron of the charge accumulation layers 4a and 4b.
Therefore, the faulty deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and faulty deletion which originates by that cause, such as the poor leakage, a poor program, and poor read-out can not be produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and highly reliable nonvolatile semiconductor memory can be realized.
It is advisable for the charge accumulation layers 4a and 4b to consist of silicon nitride of high charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer or a polycrystal silicon layer, it can be manufactured cheaply.
If the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are furthermore constituted from a silicon nitride (Si_3N_4 layer) which has a dielectric constant of about 2 times the one of a silicon oxide (SiO_2 layer), a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is about 4nm - 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion

thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection extraction operation is reduced, and not only micronization of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0030] Although n- type diffusion layer 10 is established for the purpose of the pressure-proof enhancement in a source field and a drain field and LDD structure is constituted from a memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention, a source field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4a-4b, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film which has a high dielectric constant is used for 2 gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved As a metal oxide film, there are TiO2, Ta2O5, aluminum2O5, and PZT and SBT.

[0031] Next, an operation of the non-volatile memory concerning the 2nd embodiment form of this invention is explained using the Fig. 11 and the Fig. 12 .
Fig. 11 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 12 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 11 , at the time of the writing of a memory cell, about 7-8V is impressed to gate G, about 5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field by the channel thermoelectron (CHE).
When pouring an electron into charge accumulation layer 4a by the side of a source field you just need to replace in the above-mentioned case the voltage impressed to each drain D and source S.
On the other hand, as shown in Fig. 12 , a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler-Nordheim (FN) type tunnel current.
Moreover, when the gate electrode 3 is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells.
In this case, source S and drain D should just take as the p type semiconductor substrate 1 and this potential.
Moreover, it is also possible to impress the right voltage different from the potential of the p type semiconductor substrate 1 to drain D, and to draw out an electron for source S only from floating potential (Floating), then charge accumulation layer 4a by the side of drain D.
What is necessary is to impress a right voltage to source S, in drawing out an electron only from charge accumulation layer 4b by the side of source S, and just to let drain D be floating potential.

[0032] The writing of a memory cell can also be performed like a deletion of a memory cell using FN current.
About 10V is impressed between gate G and the p type semiconductor substrate 1, and an electron is poured into the charge accumulation layers 4a and 4b with FN current.
In this case, an electron can be simultaneously poured into two or more memory cells in which have gate G in common.

[0033] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be

memorized in one cell.

[0034] Next, the manufacture technique of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention is explained using Fig. 13 through Fig. 19 .
As first shown in Fig. 13 , the small silicon nitride of charge store capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed.
Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD (Jet-Vapor-Deposition) method.
The JVD method is indicated by bibliography "T.P.Ma, IEEE Transactions ON Electron Devices, Volume 45 Number 3, and March 1998 p680."
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, the silicon nitride of small charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0035] Next, as shown in Fig. 14 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then the 1st gate insulator layer 13 of the front face of the p type semiconductor substrate 1 of the field which uses the gate electrode 3 as a mask and forms a source field and a drain field, the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 are dry-etched self-conformably.

[0036] Next, as shown in Fig. 15 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 2nd embodiment form of this invention, since it reaches 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which contains HF gas, instead of the wet etching method which used the etching reagent.

[0037] Next, as shown in Fig. 16 , it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the silicon nitride 18 of high charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
And as shown in Fig. 17 , anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of a silicon nitride of high charge store capacity are formed.

[0038] Next, as shown in Fig. 18 , after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
N- type diffusion layer 10 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0039] Next, as shown in Fig. 19 , after forming the side wall spacer 9 in the side wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
N+ type diffusion layer 11 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 and the side wall spacer 9 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0040] Next, membranes of high-melting point metals such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, and then, by heat-treating the p type semiconductor substrate 1 in an inert atmosphere, in each front face of the gate electrode 3 and n+ type diffusion layer 11 the electric conduction layer 12 which consists of a refractory-metal silicide is formed.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 10 will be completed.

[0041] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 10 , and a final nonvolatile memory cell is completed.

[0042] Thus, with the 2nd embodiment form of this invention, the charge accumulation layers 4a and 4b can be formed in a self-matching way down the ends of the gate electrode 3.
Therefore, micronization in the orientation of gate length of a cell transistor is attained.
Thereby, large capacity and high-density nonvolatile semiconductor memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and nonvolatile semiconductor memory reduced sharply can be realized.

[0043] Moreover, the width of face of the orientation of channel length of the charge accumulation layers 4a and 4b can be easily controlled by adjustment of the etch-rate difference and etching time of the 1st gate insulator layer 13, and of the 3rd gate insulator layer 15 and the 2nd gate insulator layer 14,.
Thereby, the charge accumulation layers 4a and 4b can be arranged symmetrically.
And since the charge accumulation layers 4a and 4b are electrically separated completely by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b do not happen.
Furthermore, since the charge accumulation layers 4a and 4b are insulated completely from a source field, a drain field, the gate electrode 3, and a channel field by the 1st insulator layer 13, 3rd insulator layer 15, and oxide film 16, the nonvolatile semiconductor memory with excellent charge hold property can be offered.
Charge accumulation layers 4a and 4b are formed extending in the orientation of a channel field from the edge of the gate electrode 3, and the current-conducting characteristics of a memory cell are mainly set by the charge store status of the part by the side of the channel field of the charge accumulation layers 4a and 4b.
Therefore, if the length of the orientation of gate length of this part is reduced to the limits, more detailed nonvolatile semiconductor memory can be offered.

[0044] Furthermore, since the cellular structure is easily realizable at usual CMOS process, nonvolatile semiconductor memory can be manufactured at low cost using the existing production line.

[0045] (3rd Embodiment Form) Next, the 3rd embodiment form of this invention is explained.
The 3rd embodiment form of this invention is the 2nd embodiment form shown in Fig. 10 with the silicon oxide transposed for the 1st gate insulator layer 13 and the 2nd gate insulator layer 14 are transposed to a silicon nitride, and the 3rd gate insulator layer 15 is to a silicon oxide.
Hereafter, the manufacture technique of the memory cell of the nonvolatile semiconductor memory concerning the 3rd embodiment form of this invention is explained with reference to Fig. 13 through Fig. 15.

[0046] First, as for the memory cell of the nonvolatile semiconductor memory concerning the 3rd embodiment form of this invention, the p type semiconductor substrate 1 is oxidized thermally, and the 1st gate insulator layer 13 which consists of an about 10nm silicon oxide is formed.

After 1st gate insulator layer 13 formation, the silicon nitride of the low charge store capacity is deposited by the JVD method and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, a silicon oxide is deposited by CVD and the about 10nm 3rd gate insulator layer 15 is formed (refer to the Fig. 13).

[0047] Next, after depositing the about 50-250nm polycrystal silicon layer which is doped with n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then, at the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layer 15 of the front face of the p type semiconductor substrate 1 of the field which forms a source field and a drain field using the gate electrode 3 as a mask, dry etching is carried out self-adjustingly (refer to the Fig. 14).

[0048] Next, the p type semiconductor substrate 1 is oxidized thermally, and a thin silicon oxide is formed all over p type semiconductor substrate 1.
Then, the space 17 for charge accumulation layer formation is formed.
The space 17 for this charge accumulation layer formation is formed by using the etching reagent with the large etch rate on the 2nd gate insulator layer 14 rather than on the1st gate oxide-film 13 and the 3rd gate insulator layer 15, and carrying out wet etching selectively the edge of the 2nd gate insulator layer 14.
With the 3rd embodiment form of this invention, since 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon oxide and the 2nd gate insulator layer 14 is constituted from a silicon nitride, for example a phosphoric-acid type may be used as an etching reagent.
In addition, since the silicon nitride 14 hardly oxidizes by thermal oxidation processing, an oxide film is not formed in the side face of the 2nd gate insulator layer, but, for this reason, the selectivity of etching improves (refer to the Fig. 15).
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which contains CF4 gas instead of the wet etching method which used the etching reagent.
The subsequent process is the same as the 2nd embodiment form.

[0049] (4th embodiment form) Next, the 4th embodiment form of this invention is explained. Fig. 20 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.
The 4th embodiment form of this invention is the example that constituted the memory cell from a p type MOS transistor.
As shown in Fig. 20, with the memory cell structure of the non-volatile memory concerning the 4th embodiment form of this invention, the 2nd gate insulator layer 14 is formed in the surface of the n-type-semiconductor substrate 19 through the 1st gate insulator layer 13.
The charge accumulation layers 4a and 4b are formed in the ends of 2 gate insulator layer 14.
On the 2nd gate insulator layer 14 and charge accumulation layer 4a and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and p- type diffusion layer 20 of the low impurity concentration which touches a channel field, and p+ type diffusion layer 21 of the high impurity concentration located in the outside of this p-type diffusion layer 20 are formed in the n-type-semiconductor substrate 19 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and p+ type diffusion layer 21.

[0050] Next, an operation of the non-volatile memory concerning the 4th embodiment form of this invention is explained using the Fig. 21 and the Fig. 22 .
Fig. 21 is a cross section of the non-volatile memory explaining a write-in operation.

Fig. 22 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 21 , at the time of the writing of a memory cell, about 5V is impressed to gate G, and about -5V is impressed to drain D, respectively, and let source S be floating potential.
Thus, a voltage is impressed, energy is given the electron of the tunnel phenomenon reason between band-bands by the electric field near the drain field, and an electron is poured into charge accumulation layer 4b by the side of a drain field.
The voltage impressed to drain D and source S is replaced with each other, in pouring an electron into charge accumulation layer 4a by the side of a source field.
On the other hand, as shown in Fig. 22, a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by Fig. out an electron from the charge accumulation layers 4a and 4b using FN current.
Moreover, when gate G is shared with plural cells, an electron can be simultaneously drawn out from those memory cells.
In this case, source S and drain D are taken as the n-type-semiconductor substrate 19, this potential, or floating potential.

[0051] It is possible to perform it, even if the writing of a memory cell uses a channel thermoelectron like the 2nd embodiment form of this invention.
In this case, about -2.5V is impressed to gate G, about -5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field by the channel thermoelectron.
On the other hand, just to replace the voltage impressed to drain D and source S is replaced with each other, in pouring an electron into charge accumulation layer 4a of a source field.

[0052] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current that flows between source S and drain D.
It uses that the current transfer characteristics near the source field and the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0053] (5th embodiment form) Next, the 5th embodiment form of this invention is explained.
Generally, a peripheral circuit is arranged in semiconductor memory around a memory cell array.
For example, there are a decoder, writing/deletion circuit, a readout circuitry, an analog circuit, various kinds of I/O circuits, various kinds of capacitor circuits, etc. as the peripheral circuit.
The 5th embodiment form of this invention shows the example that manufactures simultaneously the MOS transistor which constitutes these peripherals circuit using the manufacturing process of the memory cell transistor of the 2nd - the 4th embodiment form.
Fig. 23 is a cross section showing the structure of the MOS transistor that constitutes the peripheral circuit of the nonvolatile semiconductor memory concerning the 5th embodiment form of this invention.
As shown in Fig. 23 , according to the 5th embodiment form of this invention, seven kinds of MOS transistors (Tr1-Tr7) from which a gate insulator layer is different in addition to a memory cell transistor (memory cell Tr) are realizable.
In addition, the memory cell transistor of Fig. 23 is a memory cell transistor shown in Fig. 10.
Moreover, MOS transistors Tr1-Tr7 show n type MOS transistor altogether. n- type diffusion layer 10 of a memory cell transistor and n+ type diffusion layer 11, and the electric conduction layer 12 are omitted in order to make a drawing legible.
MOS transistors Tr1-Tr7 are omitted in the same way.

[0054] Next, the manufacture technique of an MOS transistor shown in Fig. 23 is explained using

the Fig. 24 or the Fig. 30.
As shown in Fig. 24 , the small silicon nitride of charge store capacity is deposited by the JVD method all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed.
Well-known exposure technique and well-known dry etching technique remove the 1st gate insulator layer 13 of the field of the part on the p type semiconductor substrate 1 after 1st gate insulator layer 13 formation.
And as shown in Fig. 25, a silicon oxide is deposited by CVD and the about 5-10nm 2nd gate insulator layer 14 is formed.
Exposure technique and dry etching technique remove the 2nd gate insulator layer 14 of a part of field after 2nd gate insulator layer 14 formation.
Then, as shown in Fig. 26 , the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
Exposure technique and dry etching technique remove the 3rd gate insulator layer 15 of a part of field after 3rd gate insulator layer 15 formation.
It does in this way and the 1st gate insulator layer 13 and seven kinds of gate insulator layers which reach 2nd gate insulator layer 14 and consist of at least one of the 3rd gate insulator layers 15 are realized.
In the above method, seven kinds of gate insulator layers are realized

[0055] Next, as shown in Fig. 27 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and plural gate electrodes 3 are formed.
Furthermore, the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and 3 gate insulator layer 15 of the surface of the p type semiconductor substrate 1 in the field which uses the gate electrode 3 as a mask and forms each source field and drain field of a memory cell transistor and an MOS transistor by dry etching, is removed.

[0056] Next, as shown in Fig. 28, the field which forms MOS transistors Tr1-Tr7 is covered by the photoresist 22, and wet etching of the field which forms a memory cell transistor is carried out.
An etching reagent uses what has an etching speed of the 2nd gate insulation film 14 quicker than the 1st gate oxidization film 13 and the 3rd gate insulation film 15.
The edge of the 2nd gate insulation film 14 of the domain that forms a memory cell transistor by this wet etching is etched alternatively, and the space 17 for electric charge accumulation layer formation is formed.
Since the 1st gate oxide film 13 and the 3rd gate insulator layer 15 are constituted from a silicone nitriding film and the 2nd gate insulation layer 14 is constituted from a silicone oxide film, for example, a fluoric acid type is used as etching reagent.
And as shown in Fig. 29, it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
Then, as shown in Fig. 30, anisotropic etching by RIE is performed to the whole surface of p type semiconductor substrate 1, and the electric charge accumulation layers 4a and 4b that consisted of high silicone nitriding films of electric charge accumulation capability are formed in the domain that forms a memory cell transistor.

[0057] According to the 5th embodiment form of this invention, seven kinds of MOS transistors Tr1-Tr7 that have the gate insulator layer with which film thickness differs can be manufactured simultaneously with a memory cell transistor.
Thereby, the MOS transistor corresponding to operating voltage various from the high pressure-proofing transistor of a high-voltage operation to a super-low voltage operation transistor can be offered.
Furthermore, it is possible to realize an n type MOS transistor and a p type MOS transistor.
Moreover, the gate electrode 3 of a memory cell transistor and MOS transistors Tr1-Tr7 consists of the same material, and is formed at the same exposure process and a dry etching process.

Therefore, it is possible to offer a detailed transistor with few position doubling gaps of a photo mask.

[0058] (6th embodiment form) Next, the 6th embodiment form of this invention is explained.
In the form of this 6th embodiment form, the example that realizes electrically the volatile memory in which writing and read-out are possible on the same tip at the non-volatility memory that can be written in and eliminated, and high speed is shown.
Fig. 31 is a sectional view showing the memory cell structure of the nonvolatile memory carried in the semiconductor memory storage concerning the 6th embodiment form of this invention.
Fig. 32 is a sectional view showing the memory cell structure of the volatile memory carried in starting-6th case of the operation of this invention semiconductor memory storage.
Non-volatile memory of Fig. 31 and volatile memory of Fig. 32 are loaded together on the same chip.

[0059] (A) As shown in non-volatile memory Fig. 31, the memory cell of the non-volatile memory concerning the 6th embodiment form consists of an n type MOS transistor.
And with the memory cell structure of this non-volatile memory, the 2nd gate insulator layer 14 is formed through the 1st gate insulator layer 13 on the principal plane of the p type semiconductor substrate 1.
The charge accumulation layer 4 (4a, 4b) is formed in the both ends of the 2nd gate insulator layer 14.
On the 2nd gate insulator layer 14 and the charge accumulation layer 4, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of gate electrode 3 and n+ type diffusion layer 11.

[0060] The memory cell of the non-volatile memory concerning the 6th embodiment form of this invention has LDD structure that constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration and an n+ type diffusion layer 11 of high impurity concentration.
And it consists of a three layer laminating films by which a gate insulator layer consists of the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer), and the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layer 4 (4a, 4b) is formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated in these two electric charge accumulation layers 4a and 4b, and the accumulation state can take the following four states.

(1) Neither of the electric charge accumulation layers 4a and 4b is accumulating the electron.
(2) Only electric charge accumulation layer 4a is accumulating the electron.
(3) Only electric charge accumulation layer 4b is accumulating the electron.
(4) The electric charge accumulation layers 4a and 4b are accumulating the electron.

The amount of change of the threshold voltage produced by the existence of the electron held at these two electric charge accumulation layers 4a and 4b is made to correspond to memory information "00", "01", "10" and "11".
Moreover, with this memory cell structure, since the charge accumulation layer 4 is located in the upper part of a channel field edge, the threshold voltage of the central part of a channel field is decided only by impurity concentration of a channel field, and it does not depend for it on the accumulation state of the electron of the charge accumulation layer 4.
Therefore, fault deletion (over-erase) by the excess and deficiency of the electron of the electric charge accumulation layer 4 is prevented, and the poor leakage resulting, a poor program, and poor read-out from fault deletion must have been produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only

by the gate voltage, and can realize highly reliable non-volatile memory.
What is necessary is for the charge accumulation layer 4 just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge holds property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0061] Although LDD structure is constituted from a memory cell of a nonvolatile memory by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4a and 4b, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film that has a high dielectric constant is used for 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
For example, it is possible to use TiO2, Ta 2O5, Al2O5, PZT and SBT as a metal oxide film.

[0062] Next, an operation of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention is explained using Fig.. 33 and Fig. 34 .
Fig. 33 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 34 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 33, at the time of the writing of a memory cell, about 7-8V is impressed to gate G, about 5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b of a drain field by the channel thermo electron (CHE).
What is necessary is just to replace the voltage impressed to each of drain and Sauce S, in pouring an electron into electric charge accumulation layer 4b of a sauce field.
On the other hand, as shown in Fig. 34, a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when plural memory cells share gate G, an electron can be simultaneously drawn out from those memory cells.
In this case, what is necessary is just to make Sauce S and drain D into the same potential as p type semiconductor substrate 1.
Moreover, if different right voltage from the potential of p type semiconductor substrate 1 is impressed to drain electrode and sauce electrode is made into floating potential (Floating), it is also possible to draw out an electron only from electric charge accumulation layer 4b of drain electrode.
What is necessary is to impress right voltage to sauce electrode, in drawing out an electron only from electric charge accumulation layer 4a of sauce electrode, and just to let drain electrode be floating potential.

[0063] The writing of a memory cell can also be performed like a deletion of a memory cell using FN current.
About 10V is impressed between gate G and the p type semiconductor substrate 1, and an

electron is poured into the charge accumulation layers 4a and 4b with FN current.
In this case, an electron can be simultaneously poured into plural memory cells in which gate G is common.

[0064] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current that flows between source S and drain D.
It uses that the current transfer characteristics near a source field and the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
The information for 2 bits is memorizable in one cell by acquiring the four different current transfer characteristics according to four accumulation states of the electric charge accumulation layers 4a and 4b.

[0065] (B) As shown in volatile-memory Fig. 32, the memory cell of the volatile memory concerning the 6th embodiment form of this invention consists of an n type MOS transistor.
With the memory cell structure of this volatile memory, the 2nd gate insulator layer 14 of Fig. 31 is directly arranged on the principal plane of the p type semiconductor substrate 1.
And although the charge accumulation layer 4 (4c, 4d) is formed in the both ends of the 2nd gate insulator layer 14 like the non-volatile memory of Fig. 31, it differs from the non-volatile memory of Fig. 31 in that these charge accumulation layers 4c and 4d are arranged on the principal plane of p type semiconductor substrate 1 through the tunnel insulation layer 23.
On the 2nd gate insulator layer 14 and the charge accumulation layer 4, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of gate electrode 3 and n+ type diffusion layer 11.

[0066] The memory cell of the volatile memory concerning the 6th embodiment form of this invention has LDD structure that constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration and an n+ type diffusion layer 11 of high impurity concentration.
And a gate insulator layer consists of the 2nd gate insulator layer 14, a tunnel insulator layer 23 and the 3rd gate insulator layer 15, and the charge accumulation layer 4 is formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated in these two electric charge accumulation layers 4c and 4d, and the accumulation state can take the following four states.

(1) Electric charge accumulation layers 4c and 4d neither is accumulating the electron.
(2) Only electric charge accumulation layer 4c is accumulating the electron.
(3) Only 4d of electric charge accumulation layers is accumulating the electron.
(4) The electric charge accumulation layers 4c and 4d are accumulating the electron.

The amount of which is produced by the existence of the electron held at these two charge accumulation layers 4c and 4d threshold change of potential is made to correspond to a storage information "00", "01", "10" and "11".
Moreover, with this memory cell structure, since the charge accumulation layer 4 is located in the upper part of the edge of a channel field, the threshold voltage of the central part of the channel field is decided only by impurity concentration of a channel field, and it does not depend for it on the accumulation state of the electron of the charge accumulation layer 4.
Therefore, the fault deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and the poor leakage, a poor program, and poor read-out which originates in a fault deletion by that cause must have been produced.

Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and can realize highly reliable volatile memory.
What is necessary is for the charge accumulation layer 4 just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
Furthermore, if the 3rd gate insulator layer 15 is constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm to about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0067] Although LDD structure is constituted from a memory cell of a nonvolatile memory by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4c and 4d, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film that has a high dielectric constant is used for 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
For example, it is possible to use TiO2, Ta 2O5, Al2O5, PZT and SBT as a metal oxide film.

[0068] In the volatile memory concerning the 6th embodiment form of this invention, the tunnel insulator layer 23 is arranged in the lower part of a charge accumulation layers 4c and 4d.
The tunnel insulator layer 23 consists of a silicon oxide of the thin film which has the thickness in which direct tunneling is possible, and makes possible high-speed read-out and write-in in 100ns or less required of a dynamic RAM.
When the tunnel insulator layer 23 is constituted from a silicon oxide, the thickness is just 3nm or less.
Moreover, if the tunnel insulator layer 23 is constituted from a silicon nitride 3nm or less, a silicon-oxide conversion thickness can realize stably the very thin gate insulator layer which is about 1.5nm.
Since the electron accumulated by the leakage current through the tunnel insulator layer 23 at the charge accumulation layer 4 decreases gradually, prolonged data-hold is difficult in practice.
However, re-writing is possible enough within the refreshment term of a usual dynamic RAM, and it is thought that it is satisfactory at all in the operation as a dynamic RAM.
This is shown in 1995 IEDM digest p.867 by C.H-J.Wann et al.

[0069] Reading of a memory cell is performed by detecting the read-out current which flows between a source electrode and drain electrodes.
It uses that the current transfer characteristics near a source field and the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4c and 4d.
To which a bias shall be carried out between source electrode and drain electrode should just choose the direction where the modulation of current transfer characteristics appears notably.
The information for 2 bits is memorizable in one cell by acquiring the four different current transfer characteristics according to four accumulation states of the electric charge accumulation layers 4c and 4d.

[0070] Furthermore, if the volatile memory concerning the 6th embodiment form of this invention does not pour a charge into the charge accumulation layers 4c and 4d, it is possible to make it operate as a usual MOS transistor.

[0071] (C) The manufacture method of a non-volatility and a volatile mixed-loading memory
Next, the manufacture method of the memory cell of the nonvolatile memory concerning the 6th embodiment form of this invention and an volatile memory is explained using Fig. 35 to Fig. 43 and using Fig. 44 to Fig. 52.
Fig. 35 to Fig. 43 are showing the manufacture method of the non-volatile memory concerning the 6th embodiment form of this invention.
Fig. 44 to Fig. 52 are showing the manufacture method of the volatile memory concerning the 6th embodiment form of this invention.

[0072] As first shown in Fig. 35 and Fig. 44, the small silicon nitride of charge store capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed.
After 1st gate insulator layer 13 formation, the non-volatile memory formation field of Fig. 35 is covered by the photoresist for example and only the 1st gate insulator layer 13 of the volatile-memory formation field of Fig. 44 is removed by the wet etching method for example, using the heating phosphoric-acid solution.
Therefore, the 1st gate insulator layer 13 is formed only in the non-volatile memory formation field of Fig. 35.
Deposition of a silicone nitriding film with small electric charge accumulation capability is performed for example, by the JVD method.

[0073] Next, as shown in the Fig. 36 and the Fig. 45 , a silicon oxide is deposited all over p type semiconductor substrate 1 by CVD, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, a silicone nitriding film with small electric charge accumulation capability is deposited by the JVD method, and the about 10nm 3rd gate insulation film 15 is formed.
After all, the 1st, the 2nd and 3rd gate insulator layers 13, 14 and 15 are formed in the non-volatile memory formation field of Fig. 36, and the 2nd and the 3 gate insulator layers 14 and 15 are formed in the volatile-memory formation field of Fig. 45.

[0074] Next, as shown in the Fig. 37 and the Fig. 46 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then, in the nonvolatile memory formation field of Fig. 37, dry etching the 1st gate insulation film 13, the 2nd gate insulation film 14 and the 3rd gate insulation film 15 on the surface of p type semiconductor substrate 1 of the field which forms a sauce filed and a drain field is carried out self-adjustingly.
On the other hand, in the volatile-memory formation field of Fig. 46 , dry etching of the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 is carried out self-adjustingly.

[0075] Next, as shown in the Fig. 38 and the Fig. 47, the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by carrying out wet etching of the end of the 2nd gate insulator layer 14 alternatively using etching liquid with an etching speed of the 2nd gate insulation film 14 quicker than the 1st gate oxide-film 13.
The space 17 to form a charge accumulation layer in the non-volatile memory formation field in the nonvolatile memory formation domain of Fig. 38 and the space 17 to form a charge accumulation layer in the volatile memory formation field in the nonvolatile memory formation domain of Fig. 47 is formed simultaneously.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 6th embodiment form of this invention, since the 1st gate oxide-film 13 and the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from

a silicon oxide.
Moreover, you may form this space 17 by the plasma dry etching method using the gas which contains HF gas instead of the wet etching method which used etching reagent.

[0076] Next, as shown in the Fig. 39 and the Fig. 48 , it oxidizes by the RTO method and the tunnel insulator layer 23 which consists of the silicon oxide in which a direct tunnel is possible is formed for the whole surface of p type semiconductor substrate 1.

[0077] Next, as shown in the Fig. 40 and the Fig. 49 , it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
And as shown in the Fig. 41 and the Fig. 50 , anisotropic etching by RIE is performed to whole surface of the p type semiconductor substrate 1, and the charge accumulation layer 4 (4a, 4b, 4c, 4d) which consisted of a silicon nitride of high charge store capacity is formed simultaneously.

[0078] Next, as shown in the Fig. 42 and the Fig. 51 , after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
It forms by activating the impurity which n- type diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technique, poured in n type impurity, and was poured in with subsequent heat treatment.

[0079] Next, as shown in the Fig. 43 and the Fig. 52 , after forming the side wall spacer 9 in the side attachment wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
It forms by activating the impurity which n+ type diffusion layer 11 used the gate electrode 3 and the side wall spacer 9 as the mask with ion-implantation technique, poured in n type impurity, and was poured in with subsequent heat treatment.

[0080] And the thing for which high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere and the electric conduction layer 12 which consists of a refractory-metal silicide is formed in each surface of the gate electrode 3 and n+ type diffusion layer 11.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure of volatile memory shown in the non-volatile memory the Fig. 32 and having shown in Fig. 31 will be completed.

[0081] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of the Fig. 31 and the Fig. 32 , and the semiconductor device which carried final non-volatile memory and final volatile memory is completed.

[0082] Thus, with the 6th embodiment form of this invention, the charge accumulation layer 4 (4a, 4b, 4c, 4d) can be formed in a self-matching target down the ends of the gate electrode 3.
Therefore, micronization of the orientation of gate length of the memory cell transistor of the Fig. 31 and the Fig. 32 is attained.
Thereby, large capacity, high-density non-volatile memory, and volatile memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and the non-volatile memory and volatile memory that were reduced sharply can be realized.

[0083] The width of the direction of channel length of the charge accumulation layer 4 is easily controllable by the etching speed difference of p type semiconductor substrate 1, the 1st gate insulation film 13, the 3rd gate insulation film 15, and the 2nd gate insulation film 14, and regulation of etching time.

Thereby, the charge accumulation layer 4 can be arranged symmetrically.
And since it is electrically separated completely by the 2nd gate insulation film 14 between the electric charge accumulation layers 4, the interaction between the electric charge accumulation layers 4 does not happen.
Furthermore, from a source field, a drain field, the gate electrode 3, and a channel field, since the 1st insulator layer 13, tunnel insulator layer 23, 3rd insulator layer 15, and oxide film 16 insulate completely, the charge accumulation layer 4 can offer the non-volatile memory and volatile memory which were excellent in the charge hold property.
The charge accumulation layer 4 is extended and formed in the direction of a channel field from the end of gate electrode 3, and the current transfer-characteristics of a memory cell is mostly decided by the electric change accumulation state of the fraction by the side of the channel field of the electric charge accumulation layer 4.
Therefore, if the length of the orientation of gate length of this fraction is reduced to a limitation, more detailed non-volatile memory and more detailed volatile memory can be offered.

[0084] Since it is easily realizable at usual CMOS process, the cellular structure can manufacture non-volatile memory and volatile memory by the low cost using the existing production line.

[0085] Furthermore, since the greater part of the manufacturing process is communalized, it is a low cost, and above-mentioned non-volatile memory and above-mentioned volatile memory are the short manufacture time necessary for completion, and can manufacture the semiconductor device consolidated with non-volatile memory and volatile memory.

[0086] In addition, although the 1st gate insulator layer 13 is constituted from silicon nitride and the 2nd gate insulator layer 14 are constituted from a silicon oxide and the 3rd gate insulator layer 15 is constituted from silicon nitride in the 6th embodiment form of this invention, you may constitute the 1st gate insulator layer 13 from a silicon oxide, the 2nd gate insulator layer 14 from a silicon nitride, and the 3rd gate insulator layer 15 from a silicon oxide.
In this case, for example, the 1st gate insulator layer 13 consists of an about 10nm silicon oxide which oxidized thermally the p type semiconductor substrate 1.
The 2nd gate insulator layer 14 consists of a low silicon nitride of the about 5-10nm-charge store capacity deposited by the JVD method.
The 3rd gate insulator layer 15 consist of an about 10nm silicon oxide deposited by CVD.
Moreover, since formation of the space 17 for charge accumulation layer formation constitutes 1st gate oxide-film 13 and constitutes the 3rd gate insulator layer 15 from a silicon oxide and constitutes the 2nd gate insulator layer 14 from a silicon nitride, it should just use for example, a phosphoric-acid type as an etching reagent.

[0087](7th Embodiment Form) Next, the 7th embodiment form of this invention is explained.
The 7th embodiment form shows the example which realizes the non-volatility memory which can be written in and eliminated electrically, and the volatile memory in which writing and read-out at high speed are possible on the same chip like the 6th embodiment form of the above.
Fig. 53 is a cross section showing the memory cell structure of the nonvolatile memory carried in the semiconductor memory storage concerning the 7th embodiment form of this invention.
Fig. 54 is a cross section showing the memory cell structure of the volatile memory carried in the semiconductor memory storage concerning the 7th embodiment form of this invention.
Non-volatile memory of Fig. 53 and volatile memory of Fig. 54 are consolidated on the same chip.
Since it is the same as that of the 6th embodiment form of the above about the non-volatile memory shown in Fig. 53, the explanation is omitted.

[0088] As shown in Fig. 54, the memory cell of the volatile memory concerning the 7th embodiment form of this invention consists of an n type MOS transistor.
And with the memory cell structure of this volatile memory, charge accumulation layer 4e is arranged through the tunnel insulator layer 23 on the principal plane of the p type semiconductor substrate 1.

On charge accumulation layer 4e, the gate electrode 3 is formed through the 4th gate insulator layer 24.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and n+ type diffusion layer 11.

[0089] The memory cell of the volatile memory concerning the 7th embodiment form of this invention has LDD structure that constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration.
And it consists of a laminated structure to which a gate insulator layer changes from the tunnel insulator layer 23 and the 4th gate insulator layer 21, and charge accumulation layer 4e is arranged between the tunnel insulator layer 23 and the 4th gate insulator layer 24.
An electron is accumulated to this charge accumulation layer 4e, and the amount of the threshold voltage produced by the existence of the electron held at this electric charge accumulation layer 4e is made to correspond to memory information "0" and "1".
What is necessary is for charge accumulation layer 4e just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge holds property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
If the 4th gate insulator layer 24 is furthermore constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm to about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, voltage at the time of electronic pouring operation and extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0090] Although LDD structure is constituted from a memory cell of a volatile memory by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.

[0091] In the volatile memory concerning the 7th embodiment form of this invention, the tunnel insulator layer 23 is arranged in the lower part of charge accumulation layer 4e.
The tunnel insulator layer 23 consists of a silicon oxide of the thin film which has the thickness in which direct tunneling is possible, and read-out write-in high-speed of it in 100 or less ns required of a dynamic RAM becomes possible.
When the tunnel insulator layer 23 is constituted from a silicon oxide, the thickness is just 3nm or less.
Moreover, if constituted from a silicon nitride 3nm or less, a silicon-oxide conversion thickness can stabilize for it and realize the very thin tunnel insulator layer 23 which is about 1.5nm.

[0092] Furthermore, if an electric charge is not poured into electric charge accumulation layer 4e, it is possible to also make it operate as a usual MOS transistor as for the volatile memory concerning the 7th embodiment form of this invention.

[0093] Next, the manufacture technique of the memory cell of the non-volatile memory and volatile memory concerning the 7th embodiment form of this invention is explained using Fig. 55 to Fig. 62, and Fig. 63 to Fig. 70 .
Fig. 55 to Fig. 62 is a cross section showing the manufacture method of the nonvolatile memory concerning the form of implementation of the 7th of this invention.
Fig. 63 to Fig. 70 is a cross section showing the manufacture method of the volatile memory concerning the 7th embodiment form of this invention.

[0094] As first shown in Fig. 55 and Fig. 63, the about 10nm 1st gate insulator layer 13 is formed by depositing the small silicon nitride of charge accumulation capability all over p type semiconductor substrate 1.
Deposition of the small silicon nitride of charge store capacity is performed by the JVD method, for example.
The about 5-10nm 2nd gate insulator layer 14 is formed by depositing a silicon oxide by the CVD method after 1st gate insulator layer 13 formation.
Then, the about 10nm 3rd gate insulator layer 15 is formed by depositing the small silicon nitride of charge accumulation capability by the JVD method.

[0095] Next, as shown in Fig. 56 and Fig. 64, after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, an gate electrode 3 is formed in the nonvolatile memory formation domain in Fig. 56 by carrying out patterning with exposure technnique and etching technnique.
Then dry etching of the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 on the surface of p type semiconductor substrate 1 of the field which forms a sauce field and a drain field by using gate electrode 3 as a mask is carried out self-adjustingly.
In the volatile memory formation field of Fig. 64, a ploycrystal silicone film, the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 are removed altogether, and the surface of p type semiconductor substrate 1 is exposed.

[0096] Next, as shown in Fig. 57, in a non-volatile memory formation field, the space 17 for charge accumulation layer formation is formed.
The space 17 for this charge accumulation layer formation is formed by carrying out wet etching of the end of the 2nd gate insulator layer 14 alternatively using etching liquid with an etching speed of the 2nd gate insulator layer 14 quicker than the 1st gate oxide-film 13 and the 3rd gate insulator layer 15.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 7th embodiment form of this invention, since it reaches 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
What is necessary is just to use for example, a fluoric acid type as etching reagent, since the 1st gate oxide-film 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the silicon oxide constitutes the 2nd gate insulator layer 14 in the 7th embodiment form of this invention.
Moreover, you may form the space 17 for charge accumulation layer system formation by the plasma dry etching method using the gas which changes to the wet etching method which contains HF gas instead of the wet etching method which used etching reagent.On the other hand, as shown in Fig. 65, in the volatile-memory formation field, the surface of the p type semiconductor substrate 1 has been exposed.

[0097] Next, as shown in Fig. 58 and Fig. 66, the tunnel insulator layer 23 which is by the RTO method for example, and consists of the silicon oxide which can be tunneled direct is formed all over p type semiconductor substrate 1.
After forming the tunnel insulation film 23, the silicon nitride 18 of high electric charge accumulation capability is deposited by the LPCVD method all over p type semiconductor substrate 1.

At this time, the space 17 for electric charge accumulation layer formation is completely embedded with the silicone nitriding film 18.
And as shown in Fig. 59, in a nonvolatile memory formation field, anisotropic etching by RIE is performed to the whole surface of p type semiconductor board 1, and the electric charge accumulation layer 4 (4a, 4b) which consisted of high silicon nitride 18 of electric charge accumulation capability is formed.
In that case, the volatile memory formation field shown in Fig. 67 is covered by photoresist, and the silicone nitride 18 is not etched.

[0098] After etching the silicon nitride 18, a silicon oxide is deposited all over p type semiconductor substrate 1, and the 4th gate insulator layer 24 is formed.
In this time the 4th gate insulator layer 24 of the nonvolatile memory formation field shown in Fig. 59 is removed.
The removal covers the volatile memory formation field shown in Fig. 67 by photoresist, and is performed by etching the 4th gate insulator layer 24 deposited on the nonvolatile memory formation field shown in Fig. 59.

[0099] Next, as shown in Fig. 68, the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method accumulates all over p type semiconductor substrate 1.
And patterning of the polycrystal silicon layer is carried out with exposure technique and etching technique, and gate electrode 3a is formed.
Then, using gate electrode 3a be an etching mask, dry etching of the tunnel insulator layer 23, electric charge accumulation layer 4e and the 4th gate insulator layer 24 on the surface of p type semiconductor substrate 1 of the field which forms a sauce field and a drain field is carried out self-adjustingly.
On the other hand, in a nonvolatile memory formation field, as shown in Fig. 60, all plycrystal silicone films may be removed, or patterning may be carried out according to gate electrode 3, and new gate electrode may be formed.

[0100] Next, as shown in the Fig. 61 and the Fig. 69 , after pouring in n type impurities by using the gate electrode 3 as a mask with ion implantation technique, n- type diffusion layer 10 is formed by activating the impurity poured in by heat treatment.

[0101] Next, as shown in the Fig. 62 and the Fig. 70 , after forming the side wall spacer 9 in the side wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
After pouring in n type impurity with ion implantation technique by using the gate electrode 3 and the sidewall spacer 9 as a mask, n+ type diffusion layer 11 is formed by activating the impurities poured in by heat treatment.

[0102] Next, high-melting point metal membranes, such as tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter method all over the p type semiconductor substrate 1 and the electric conduction layer 12 which consists of refractory metal silicide is formed on each surface of the gate electrode 3 and n+ type diffusion layer 11 by heat-treating p type semiconductor substrate 1 in an inactive atmosphere.
After the electric conduction layer 12 was formed, if the unreacted high-melting point metal which remained in fields other than the above is removed, the memory cell structure of a nonvolatile memory shown in Fig. 53 and of a volatile memory shown in Fig. 54 will be completed.

[0103] Although illustration is not carried out, after memory cell structure completion of Fig. 53 and Fig. 54, a final non-volatility memory cell and an volatile memory cell are completed through the usual CMOS manufacturing processes, such as an insulator-layer formation process between layers, a contact hole formation process, a wiring formation process and a passivation film formation process, one by one.

[0104] With the 7th embodiment form of this invention, although the 1st gate insulator layer 13 consists of silicon nitride, the 2nd gate insulator layer 14 consists of silicon oxide and the 3rd gate insulator layer 15 consists of silicon nitride, the 1st gate insulator layer 13 may be constituted from a silicon oxide, the 2nd gate insulator layer 14 may be constituted from a silicon nitride, and the 3rd gate insulator layer 15 be constituted from a silicon oxide.
In this case, for example, the 1st gate insulator layer 13 consists of an about 10nm silicon oxide which oxidized thermally the p type semiconductor substrate 1.
The 2nd gate insulator layer 14 consists of a low silicon nitride of the about 5-10nm charge store capacity deposited by the JVD method.
The 3rd gate insulator layer 15 consists of an about 10nm silicon oxide deposited by CVD.
Moreover, what is necessary is just to use for example, a phosphoric-acid type as an etching reagent in formation of the space 17 for electric charge accumulation layer formation, since the 1st gate oxide-film 13 and the 3rd gate insulator layer 15 are constituted from a silicon oxide and the 2nd gate insulator layer 14 is constituted from a silicon nitride.

[0105] Although both the memory cells of non-volatile memory and volatile memory explained the example which consists of an n type MOS transistor with the gestalt of the 6th and operation of the 7th of this invention, of course, you may be the memory cell of p type MOS transistor of an opposite conductivity type.
In this case, what is necessary is just to read the electric conduction type of a substrate or a diffusion layer as an opposite thing suitably in the above-mentioned explanation.

[0106] (8th Embodiment Form) Next, the 8th embodiment form of this invention is explained.
In the above 1st to the 7th embodiment forms, the structure of a charge accumulation layer is not directly contributed to the enhancement in electron-injection efficacy.
In the nonvolatile semiconductor memory of floating-gate structure, a stage is prepared in a channel fraction and the attempt which raises electron-injection efficacy is proposed. (S. Ogura and 1998 IEDM, p987, and the U.S. patent number of No. 5780341)
However, this proposal is weak to the defect and leak site in an oxidization film in order to adopt floating gate structure.
Moreover, there is a possibility that sufficient reliability cannot be acquired, also to the defect which may be generated at the time of stage structure formation.
The 8th embodiment form of this invention is an easy process, and can raise electron-injection efficacy.

[0107] Fig. 71 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.
This 8th embodiment form aims at enhancement in the electron-injection efficacy at the time of writing by the method of preparing a stage and an inclination in the channel field of a memory cell.
As shown in Fig. 71 , this memory cell consists of an n type MOS transistor.
And with the structure of the memory cell concerning the 8th embodiment form, the 2nd gate insulator layer 14 is formed on the surface of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
The charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14.
On the 2nd gate insulator layer 14 and charge accumulation layer 4a and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15.
The side wall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this side wall spacer 9.
The electric conduction layer 12 is formed on each surface of the gate electrode 3 and n+ type diffusion layer 11.

[0108] Furthermore, with the memory cell structure of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention, a stage 26 is formed in the channel field 25.
With this stage 26, the charge accumulation layer 4 will be located in the dispersion orientation of the electron in the p type semiconductor substrate 1.
Therefore, the injection efficiency of the electron at the time of writing improves.

[0109] The memory cell of the non-volatility semiconductor memory concerning the 8th embodiment form of this invention has the LDD structure where the sauce field and the drain field consisted of an n- type diffusion layer 10 of low impurities concentration and an n+ type diffusion layer 11 of high impurities concentration.
A gate insulator layer consists of three-layer laminating films which consist of the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer) and the 3rd gate insulator layer 15 (upper layer), and the electric charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated to these two charge accumulation layers 4a and 4b, and the accumulation state can take the following four status.
(1) The state where neither of the electric charge accumulation layers 4a and 4b is accumulating the electron,
(2) The state where only electric charge accumulation layer 4a is accumulating the electron,
(3) The state where only electric charge accumulation layer 4b is accumulating the electron,
(4) The state where the electric charge accumulation layers 4a and 4b are accumulating the electron,
The amount of which is produced by the existence of the electron held at these two charge accumulation layers 4a and 4b threshold change of potential is made to correspond to a storage information "00", "01", "10" and "11".
Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located in the upper part of a channel field edge, the threshold voltage of the central part of a channel field is decided only by impurity concentration of a channel field, and it does not depend for it on the accumulation state of the electron of the charge accumulation layers 4a and 4b.
Therefore, fault deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and the poor leakage, a poor program, and poor read-out resulting from fault deletion must have been produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and can realize highly reliable nonvolatile semiconductor memory.
What is necessary is for the charge accumulation layers 4a and 4b just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) dielectric constant, a silicon-oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out.
Therefore, the voltage at the time of an electronic injection extraction operation is formed into low voltage, and not only detailed-izing of a memory cell but micronization of a circumference high-voltage operation element of it is attained.

[0110] Although LDD structure is constituted from a memory cell of a nonvolatile memory concerning the 8th embodiment form of this invention by installing n- type diffusion layer 10 for the purpose of pressure-proof enhancement of a sauce field and a drain field, a sauce field and a drain field may consist of single drain structure and double drain structure.

Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layer 4a and 4b, it can consist of a silicon oxide, for example.
Moreover, if the metal oxide film that has a high dielectric constant is used for 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
For example, it is possible to use TiO2, Ta 2O5, Al2O5, PZT and SBT as a metal oxide film.

[0111] With the 8th embodiment form of this invention, although the stage 26 was formed in both of the source and a drain, you may prepare only in either.
Especially the memory that memorizes the information for 1 bit is enough if there is only one.

[0112] Next, an operation of the non-volatile memory concerning the 8th embodiment form of this invention is explained using Fig. 72 and Fig. 73.
Fig. 72 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 73 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 72 , at the time of the writing of a memory cell, about 6-8V is impressed to gate G, about 4-5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b of the drain field by the channel thermoelectron (CHE).
By having formed the stage 26 in the channel field 25, it is located in the electronic dispersion orientation at charge accumulation layer 4b.
For this reason, the electronic injection efficiency to charge accumulation layer 4b can improve, and improvement in the speed of an injection speed and reduction-ization of applied voltage can be attained.
What is necessary is just to replace with the above-mentioned case the voltage impressed to drain D and each source S, in pouring an electron into charge accumulation layer 4a of a source field.
On the other hand, as shown in Fig. 73 , a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when the gate electrode 3 is shared by plural memory cells, an electron can be simultaneously drawn out from those memory cells.
In this case, Sauce S and Drain D should just be taken as the same potential as p type semiconductor substrate 1.
Moreover, it is also possible to impress the right voltage different from the potential of the p type semiconductor substrate 1 to drain D, and to draw out an electron for source S only from floating potential (Floating), then charge accumulation layer 4a of drain D.
What is necessary is to impress a right voltage to source S, in drawing out an electron only from charge accumulation layer 4b of source S, and just to let drain D be floating potential.

[0113] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between source S and drain D.
It uses that the current transfer characteristics near the source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0114] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 8th embodiment form of this invention is explained using the Fig. 74 to the Fig. 82.
As first shown in Fig. 74, the wrap photoresist pattern 27 is formed for the field in which the channel field 25 is formed on the p type semiconductor substrate 1.
And as shown in Fig. 75, a stage 26 is formed by etching the p type semiconductor substrate 1

by the RIE method.

[0115] Next, as shown in Fig. 76, the small silicon nitride of charge store capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD method.
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0116] Next, as shown in Fig. 77, after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then dry etching of the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3rd gate Insulator layer 15 on the surface of p type semiconductor substrate 1 of the field which forms a sauce field and a drain field by using the gate electrode 3 as a mask is carried out self-adjustingly.

[0117] Next, as shown in Fig. 78 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 alternatively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14.
This space 17 is formed by carrying out wet etching of the end of the 2nd gate insulator layer 14 alternatively using etching liquid with an etching speed of the 2nd gate insulation film 14 quicker than the 1st gate oxide-film 13.
What is necessary is just to use for example, a fluoric acid type as an etching reagent with the 8th embodiment form of this invention, since the 1st gate oxidization film 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which contains HF gas instead of the wet etching method which used the etching reagent.

[0118] Next, as shown in Fig. 79, it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over p type semiconductor substrate 1.
And as shown in Fig. 80, anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of a silicon nitride of high charge store capacity are formed.

[0119] Next, as shown in Fig. 81 , after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
N- type diffusion layer 10 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0120] Next, as shown in Fig. 82, after forming the side wall spacer 9 in the side attachment wall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
N+ type diffusion layer 11 is formed by pouring in n type impurity with ion-implantation technique which uses the gate electrode 3 and the side wall spacer 9 as the mask, and by activating the impurity that was poured in with subsequent heat treatment.

[0121] Next, membranes of high-melting point metals such as a tungsten, titanium, and cobalt,

are deposited by CVD or the spatter all over the p type semiconductor substrate 1, and then, by heat-treating the p type semiconductor substrate 1 in an inert atmosphere, in each front face of the gate electrode 3 and n+ type diffusion layer 11 the electric conduction layer 12 which consists of a refractory-metal silicide is formed.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 71 will be completed.

[0122] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 71 , and a final nonvolatile memory cell is completed.

[0123] Thus, with the 8th embodiment form of this invention, the charge accumulation layers 4a and 4b can be formed in a self-matching way down the ends of the gate electrode 3.
Therefore, micronization in the orientation of gate length of a cell transistor is attained.
Thereby, large capacity and high-density nonvolatile semiconductor memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and nonvolatile semiconductor memory reduced sharply can be realized.

[0124] Moreover, the width of face of the orientation of channel length of the charge accumulation layers 4a and 4b can be easily controlled by adjustment of the etch-rate difference and etching time of the 1st gate insulator layer 13, and of the 3rd gate insulator layer 15 and the 2nd gate insulator layer 14.
Thereby, the charge accumulation layers 4a and 4b can be arranged symmetrically.
And since the charge accumulation layers 4a and 4b are electrically separated completely by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b do not happen.
Furthermore, since the charge accumulation layers 4a and 4b are insulated completely from a source field, a drain field, the gate electrode 3, and a channel field by the 1st insulator layer 13, 3rd insulator layer 15, and oxide film 16, the nonvolatile semiconductor memory with excellent charge hold property can be offered.
Charge accumulation layers 4a and 4b are formed extending in the orientation of a channel field from the edge of the gate electrode 3, and the current-conducting characteristics of a memory cell are mainly set by the charge store status of the part by the side of the channel field of the charge accumulation layers 4a and 4b.
Therefore, if the length of the orientation of gate length of this part is reduced to the limits, more detailed nonvolatile semiconductor memory can be offered.

[0125] Furthermore, since the cellular structure is easily realizable at usual CMOS process, nonvolatile semiconductor memory can be manufactured at low cost using the existing production line.

[0126] And with the 8th embodiment form of this invention, the electron-injection efficacy at the time of writing can be raised.
For this reason, improvement in the speed of drawing speed and reduction-ization of the applied voltage at the time of writing can be attained.

[0127] (9th Embodiment Form) Next, the 9th embodiment of this invention is explained.
In the above 8th embodiment, the 9th embodiment of this invention makes unnecessary the 2nd insulator layer 14 arranged between charge accumulation layer 4a of Fig. 71 , and charge accumulation layer 4b, and has taken the configuration which made two charge accumulation layers 4a and 4b unify.
Fig. 83 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 9th embodiment of this invention. As shown in Fig. 83 , this memory cell

structure is arranged charge accumulation layers 4f instead of to the charge accumulation layers 4a and 4b and the 2nd insulator layer 14 of the 8th embodiment.

[0128] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 9th embodiment of this invention is explained using the Fig. 84 to the Fig. 89 .
Like the 8th embodiment, as shown in Fig. 84 , the photo resist pattern 27 is formed for the field in which the channel field 25 is formed on the p type semiconductor substrate 1.
And as shown in Fig. 85 , a level difference 26 is formed by etching the p type semiconductor substrate 1 by the RIE method.

[0129] Next, as shown in Fig. 86, the silicon nitride film of small charge store capacity is deposited all over p type semiconductor substrate 1, and the 1st gate insulator layer 13 having about 10nm is formed.
Deposition of the silicon nitride film of small charge store capacity is performed for example, by the JVD method.
The silicon nitrides film 18 high of charge store capacity is formed in about 5-10nm by the LPCVD method after 1st gate insulator layer 13 formation.
Then, the silicon nitride film of small charge store capacity is deposited by the JVD method, and the 3rd gate insulator layer 15 in about 10nm is formed.

[0130] Next, as shown in Fig. 87 , after depositing the about 50-250nm polycrystal silicon layer which doped n type or p type impurity by the LPCVD method all over p type semiconductor substrate 1, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then, dry etching carried out conformably to the 1st gate insulator layer 13, the silicon nitride film 18 and the 3rd gate insulating film 15, of the surface of the p type semiconductor substrate 1 of the field, in which the source region, and drain region are formed using the gate electrode 3 as a mask, here, charge accumulation layers 4f is formed.

[0131] Next, as shown in Fig. 88, after forming an oxide film 16 all over p type semiconductor substrate 1, n- type diffusion layer 10 of low impurity concentration is formed.
Pouring n-type impurity with the gate electrode 3 as the mask with ion-implantation technique, then by activating the poured impurity with heat treatment, forms the n-type diffusion layer 10.

[0132] Next, as shown in Fig. 89, after forming the sidewall spacer 9 in the sidewall of the gate electrode 3, n+ type diffusion layer 11 of high impurity concentration is formed.
The n+ type diffusion layer 11is formed by pouring n type impurity using the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique and by activating the poured impurity by heat treatment.

[0133] Next, the high-melting point metal film, such as tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere, thereby forming the which consists of a refractory-metal silicide on the each surface of the gate electrode 3 and n+ type diffusion layer 11.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 83 will be completed.

[0134] In addition, although illustration is not shown, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 83 , and a final nonvolatile memory cell is completed.

[0135] (10th Embodiment Form) Next, the 10th embodiment of this invention is explained. Fig. 90

is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention.
In the above 8th and 9th embodiments, a level difference is prepared in the ends of a channel field by making a channel field into the concave status to a semiconductor substrate. In the 10th embodiment, a level difference is prepared in a channel field by making a channel field into the convex status to a semiconductor substrate.
And this 10th embodiment also aims at enhancement in the electron-injection luminous efficacy at the time of writing by preparing a level difference and an inclination in the channel field of a memory cell.

[0136] As shown in Fig. 90 , this memory cell consists of a p type MOS transistor. And in the structure of the memory cell concerning the 10th embodiment, the 2nd gate insulator layer 14 is formed in the surface of the n-type-semiconductor substrate 19 through the 1st gate insulator layer 13.
The charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14.
The gate electrode 3 is formed on the 2nd gate insulator layer 14 and charge accumulation layer 4a, and 4b through the 3rd gate insulator layer 15.
The sidewall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16.
The p- type diffusion layer 20 of the low impurity concentration which touches a channel field, and p+ type diffusion layer 21 of the high impurity concentration located in the outside of this p- type diffusion layer 20 are formed in the n-type-semiconductor substrate 19 of the lower part of this sidewall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and p+ type diffusion layer 21.

[0137] Furthermore, in the memory cell structure of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention, a level difference 26 is formed in the channel field 25.
Owing to this level difference 26, the charge accumulation layer 4 is located in the dispersion orientation of the electron in the p type semiconductor substrate 1. Therefore, the injection efficiency of the electron at the time of writing improves.

[0138] The memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention has LDD structure in which the source field and the drain field are constituted of a p- type diffusion layer 20 of low impurity concentration and a p+ type diffusion layer 21 of high impurity concentration.
And a gate insulator layer consists of a three-layered film, i.e. the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer) and the 3rd gate insulator layer 15 (upper layer). The charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14.
An electron is accumulated to these two charge accumulation layers 4a and 4b.
The state of accumulation can be four status:
(1) no electron is accumulated to charge accumulation layer 4a or 4b;
(2) the electron is accumulated to charge accumulation layer 4a only;
(3) the electron is accumulated to charge accumulation layer 4b only;
(4) the electron is accumulated to charge both accumulation layers 4a and 4b.
The amount of change of the threshold voltage which is produced by the existence of the electron held at these two charge accumulation layers 4a and 4b corresponds to the storage information "00", "01", "10", and "11".
Moreover, in this memory cell structure, since the charge accumulation layers 4a and 4b are located in the upper part of a channel field edge, the threshold voltage of the center of a channel field is decided only by impurity concentration of a channel field, and it does not depend on the accumulation status of the electron of the charge accumulation layers 4a and 4b.
Therefore, the fault deletion (over-erase) due to the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and the poor leakage, a poor program, and

poor read-out, which are caused in a fault deletion, never produced.
Moreover, only the gate voltage, thereby realizing highly reliable nonvolatile semiconductor memory, can suppress the leakage current between a source field and a drain field.
The charge accumulation layers 4a and 4b can be constituted of silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membranous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted of a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
If the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are furthermore constituted of a silicon nitride (Si3N4 layer) which has an about 2 times of a silicon oxide (SiO2 layer) in dielectric constant, the very thin gate insulator layer which is 4nm - about 11nm in silicon-oxide conversion thickness can be stabilized.
For example, since the real thickness of the silicon nitride whose silicon-oxide conversion thickness is 5nm is about 10nm, the induction of the direct tunnel (DT) injection is not carried out. Therefore, the voltage at the time of an electronic injection/extraction operation is lowered in battery, and not only a memory cell but also a circumference high-voltage operation element can be miniaturized.

[0139] Although p- type diffusion layer 20 is established for the purpose of the pressure-proof enhancement in a source field and a drain field and LDD structure is constituted from a memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment of this invention, a source field and a drain field may consist of single drain structure and double drain structure.
Although the 2nd gate insulator layer 14 prevents the leakage between charge accumulation layers 4a and 4b, it can consist of a silicon oxide, for example.
If the metal oxide film, which has a high dielectric constant, is used for the second gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved.
As a metal oxide film, there are TiO2, Ta2O5, aluminum2O5, and PZT and SBT.

[0140] In the 10th embodiment of this invention, the level difference 26 was formed in both by the side of the source and a drain, you may prepare only in either.
Especially the memory that memorizes the information for 1 bit is enough if there is only one side.

[0141] Next, an operation of the non-volatile memory concerning the 10th embodiment of this invention is explained using the Fig. 91 and the Fig. 92 .
Fig. 91 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 92 is a cross section of the non-volatile memory explaining a deletion operation.
As shown in Fig. 91, at the time of the writing of a memory cell, voltage of about 5V is impressed to gate G, and voltage of about -5V is impressed to drain D, respectively, and let source S be floating potential.
Thus, a voltage is impressed, energy is given the electron of the tunnel phenomenon reason between band-bands by the electric field near the drain, and it pours into charge accumulation layer 4b by the side of a drain field.
By having formed the level difference 26 in the channel field 25, charge accumulation layer 4b is located in the electronic injection orientation. For this reason, the electronic injection efficiency to charge accumulation layer 4b can improve, and improvement in the speed of an injection speed and reduction of applied voltage can be attained.
When pouring an electron into charge accumulation layer 4a by the side of a source, the voltage impressed to drain D and each source S is replaced with the above-mentioned case.
A memory cell is deleted by impressing a negative voltage (at least -5V) to gate G, as shown in Fig 92. and by drawing out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when two or more memory cells share the gate electrode 3, an electron can be simultaneously drawn out from those memory cells.

In this case, source S and drain D should just be taken as the n-type-semiconductor substrate 19 and this potential.
Moreover, if the right voltage different from the potential of the p type semiconductor substrate 1 is impressed to drain D and source S is used for floating potential (Floating), electron can be drawn out of charge accumulation layer 4a by the side of drain D.
If an electron is drawn out of only from charge accumulation layer 4b by the side of source S, a right voltage is impressed to source S and just to let drain D be floating potential.

[0142] Moreover, although illustration is not shown, read-out of a memory cell is performed by detecting the read-out current flowing between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) change according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out should be selected from the source S or drain D where the modulation of current transfer characteristics appears notably.
According to four accumulation status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0143] Next, the method of manufacturing the memory cell of the non-volatile memory concerning the 10th embodiment of this invention is explained using the Fig. 93 to Fig. 101.
As first shown in Fig. 93 , the photo-resist pattern 27 is formed on the n-type-semiconductor substrate 19 except the field in which the channel field 25 is formed.
As shown in Fig. 94, etching the n-type-semiconductor substrate 19 by the RIE method forms a level difference 26.

[0144] Next, as shown in Fig. 95, the silicon nitride of small charge store capacity is deposited all over n-type-semiconductor substrate 19, and the 1st gate insulator layer 13 having about 10nm is formed.
Deposition of the silicon nitride film of small charge store capacity is performed for example, by the JVD method.
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the 2nd gate insulator layer 14 having about 5-10nm is formed.
Then, the silicon nitride of small charge store capacity is deposited by the JVD method, and the 3rd gate insulator layer 15 having about 10nm is formed.

[0145] Next, as shown in Fig. 96 , after depositing polycrystal silicon layer having the about 50-250nm in which n type or p type impurity is doped all over n-type-semiconductor substrate 19 by the LPCVD method, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then dry etching is carried out conformably to the 1st gate insulator layer 13, the 2nd gate insulator layer 14 and the 3 rd gate insulator layer 15 of the surface of the n-type-semiconductor substrate 19 of the field which uses the gate electrode 3 as a mask and forms a source field and a drain field.

[0146] Next, as shown in Fig. 97 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 alternatively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14. In the 10th embodiment of this invention, the 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide, and a fluoric acid system, for example, can be used as an etching reagent.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas containing HF gas instead of using the wet etching method which used the etching reagent.

[0147] Next, as shown in Fig. 98 , the silicon nitride 18 of high charge store capacity is accumulated all over n-type-semiconductor substrate 19 so that the space 17 for charge accumulation layer formation can be completely embedded by the LPCVD method.
And as shown in Fig. 99, anisotropic etching by RIE is performed to the whole surface of the n-type-semiconductor substrate 19, and the charge accumulation layers 4a and 4b which consisted of a silicon nitride of high charge store capacity are formed.

[0148] Next, as shown in Fig. 100, after forming an oxide film 16 all over n-type-semiconductor substrate 19, p- type diffusion layer 20 of low impurity concentration is formed. p- type diffusion layer 20 is formed by pouring p type impurity using the gate electrode 3 as the mask with ion-implantation technique and by activating the poured impurity with heat treatment.

[0149] Next, as shown in Fig. 101, after forming the sidewall spacer 9 in the sidewall of the gate electrode 3, p+ type diffusion layer 21 of high impurity concentration is formed.
The p+ type diffusion layer 21 is formed by pouring p type impurity using the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0150] Next, a high melting point metal film such as a tungsten, titanium and cobalt, is accumulated in the whole surface of the n type semiconductor circuit board 19, by the CVD or the spatter, then the electric conduction layer 12 composed of high melting point metal silicide is formed in each surface of the gate electrode 3 and the p+ type diffusion layer 21 by a n type semiconductor circuit board 19 being subjected to heat treatment in the inert atmosphere. If the high melting point metals of the un-response left in the territory except for the above is removed after the electric conduction layer 12 formation, the memory cell structure shown in the Fig. 90 can be completed.

[0151] In addition, although illustration is not shown, usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 90, and a final nonvolatile memory cell is completed.

[0152] Thus, in the 10th embodiment of this invention, the charge accumulation layers 4a and 4b can be formed in a self-matching target down the ends of the gate electrode 3.
Therefore, miniaturization of the orientation of gate length of a cell transistor is attained.
Thereby, large capacity and high-density nonvolatile semiconductor memory can be offered.
Moreover, the cell area per bit is mostly reduced by half compared with the former, and nonvolatile semiconductor memory reduced sharply can be realized.

[0153] Moreover, the width of the charge accumulation layers 4a and 4b in the orientation of channel length can be easily controlled by adjustment of the etch-speed difference and etching time of the 1st gate insulator layer 13, the 3rd gate insulator layer 15 and the 2nd gate insulator layer 14.
Thereby, the charge accumulation layers 4a and 4b can be arranged symmetrically.
And since the charge accumulation layers 4a and 4b are electrically separated completely by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b do not happen.
Furthermore, since the charge accumulation layers 4a and 4b are insulated completely from a source field, a drain field, the gate electrode 3, and a channel field by the 1st insulator layer 13 and the 3rd insulator layer 15, and the oxide film 16, the nonvolatile semiconductor memory which was excellent in the charge hold property can be provided.
The charge accumulation layers 4a and 4b are formed in the orientation of a channel field from the edge of the gate electrode 3 and the current transfer-characteristics of the memory cell is almost decided by the charge store status of the side portion of the channel field of the charge accumulation layers 4a and 4b.
Therefore, if the length of the orientation of gate length of this portion is reduced to a limitation,

more detailed nonvolatile semiconductor memory can be provided.

[0154] Furthermore, since the cell structure is easily realizable at usual CMOS process, the nonvolatile semiconductor memory can be manufactured by the low cost using the existing production line.

[0155] And with the 10th embodiment of this invention, the electron-injection luminous efficacy at the time of writing can be raised.
For this reason, improvement in the speed and reduction of the applied voltage at the time of writing can be attained.

[0156](11th Embodiment Form) Next, the 11th embodiment form of this invention is explained.
In the 10th embodiment form of the above, the 11th embodiment of this invention makes unnecessary the 2nd insulator layer 14 arranged between charge accumulation layer 4a of Fig. 90, and charge accumulation layer 4b, and has taken the configuration which made two charge accumulation layers 4a and 4b unify.
Fig. 102 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 11th embodiment of this invention.
As shown in Fig. 102 , this memory cell structure is changed to the charge accumulation layers 4a and 4b of the 10th embodiment form of the above, and the 2nd insulator layer 14, and arranges charge accumulation layers 4f.

[0157] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 11th embodiment of this invention is explained using the Fig. 103 to the Fig. 108 .
Like the 10th embodiment of the above, as first shown in Fig. 103 , the photo resist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19.
And as shown in Fig. 104, a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.

[0158] Next, as shown in Fig. 105 , the small silicon nitride of charge store capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed.
Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD method.
About 5-10nm of the high silicon nitrides 18 of charge store capacity is formed by the LPCVD method after 1st gate insulator layer 13 formation. Then, the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0159] Next, as shown in Fig. 106 , after depositing the polycrystal silicon layer having about 50 - 250nm in which n type or p type impurity is doped by the LPCVD method all over n-type-semiconductor substrate 19, patterning is carried out with exposure technique and etching technique, and the gate electrode 3 is formed.
Then dry etching is carried out conformably to the 1st gate insulator layer 13, the silicon nitride 18, and the 3rd gate insulator layer 15, of the surface of the n-type-semiconductor substrate 19 of the field which uses the gate electrode 3 as a mask and forms a source field and a drain field.
Here, charge accumulation layer 4f is formed.

[0160] Next, as shown in Fig. 107, after forming an oxide film 16 all over n-type-semiconductor substrate 19, p- type diffusion layer 20 of low impurity concentration is formed.
The p- type diffusion layer 20 is formed by pouring p type impurity using the gate electrode 3 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0161] Next, as shown in Fig. 108, after forming the sidewall spacer 9 in the side attachment wall

of the gate electrode 3, of high impurity concentration is formed.
The p+ type diffusion layer 21 is formed by pouring p type impurity using the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0162] Next, high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere, thereby forming the electric conduction layer 12 which consists of a refractory-metal siliside on each surface of the gate electrode 3 and p+ type diffusion layer 21.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 102 will be completed.

[0163] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 102 , and a final nonvolatile memory cell is completed.

[0164] (12th Embodiment Form) Next, the 12th embodiment form of this invention is explained. Fig. 109 is a cross section showing the structure of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.
Although exposure technique and etching technique were used for patterning of the gate electrode 3 with the 10th embodiment of the above, it is the example which uses the chemical mechanical grinding method for patterning of the gate electrode 3 in the 12th embodiment.

[0165] Next, the manufacture technique of the memory cell of the non-volatile memory concerning the 12th embodiment form of this invention is explained using the Fig. 110 to the Fig. 118 . As first shown in Fig. 110 , the photoresist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19.
And as shown in Fig. 111 , a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.

[0166] Next, as shown in Fig. 112 , the small silicon nitride of charge store capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed.
Deposition of the small silicon nitride of charge store capacity is performed for example, by the JVD method.
A silicon oxide is deposited by CVD after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed.
Then, the small silicon nitride of charge store capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
Furthermore, the about 50-500nm polycrystal silicon layer 28 which doped n type or p type impurity by the LPCVD method all over n-type-semiconductor substrate 19 is deposited.

[0167] Next, as shown in Fig. 113 , the gate electrode 3 is formed by embedding the polycrystal silicon layer 19 by the chemical mechanical polishing technique. In addition, wet etching usually removes the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layer 15 which remain on the n-type-semiconductor substrate 19.

[0168] Next, as shown in Fig. 114 , the space 17 for charge accumulation layer formation is formed.
This space 17 is formed by reaching 1st gate oxide-film 13 and carrying out wet etching of the edge of the 2nd gate insulator layer 14 alternatively rather than the 3rd gate insulator layer 15 using the etching reagent with the large etch rate of the 2nd gate insulator layer 14.

What is necessary is just to use for example, a fluoric acid system as an etching reagent with the 12th embodiment form of this invention, since it reaches 1st gate oxide-film 13, the 3rd gate insulator layer 15 is constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from a silicon oxide.
Moreover, you may form the space 17 for charge accumulation layer formation by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.

[0169] Next, as shown in Fig. 115 , it deposits so that the space 17 for charge accumulation layer formation may be completely embedded in the high silicon nitride 18 of charge store capacity by the LPCVD method all over n-type-semiconductor substrate 19.
And as shown in Fig. 116 , anisotropic etching by RIE is performed to the n-type-semiconductor substrate 19 whole surface, and the charge accumulation layers 4a and 4b which consisted of a high silicon nitride of charge store capacity are formed.

[0170] Next, as shown in Fig. 117 , after forming an oxide film 16 all over n- type semiconductor substrate 19, p- type diffusion layer 20 of low impurity concentration is formed. It forms by activating the impurity which p- type diffusion layer 20 used the gate electrode 3 as the mask with ion-implantation technique, poured in p type impurity, and was poured in with subsequent heat treatment.

[0171] Next, as shown in Fig. 118 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, p+ type diffusion layer 21 of high impurity concentration is formed.
The p+ type diffusion layer 21 is formed by pouring p type impurity using used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technique, and by activating the poured impurity with heat treatment.

[0172] Next, the thing for which high-melting point metal membranes, such as a tungsten, titanium, and cobalt, are deposited by CVD or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere. Thereafter the electric conduction layer 12 which consists of a refractory-metal silicide is formed on each surface of the gate electrode 3 and p+ type diffusion layer 21.
After electric conduction layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in Fig. 109 will be completed.

[0173] In addition, although illustration is not carried out, it passes through usual CMOS manufacturing processes, such as a layer insulation layer formation process, a contact hole formation process, a wiring formation process, and a passivation layer formation process, one by one after memory cell structure completion of Fig. 109 , and a final nonvolatile memory cell is completed.

[0174] (13th Embodiment Form) Next, the 13th embodiment form of this invention is explained.
With the embodiment of the above-mentioned 1st to the 12th above-mentioned embodiment, sufficient study to improvement in the speed of transistors other than a memory cell was not made.
On the other hand, as structure of a high-speed CMOS transistor, by forming the notch on concave between a gate electrode and a source drain diffusion layer, the capacity between a gate electrode and a diffusion layer is reduced, and the attempt, which accelerates the logic gate, is made (T.Ghani et al., IEDM99, and p415).
In this 13th embodiment form, this structure is used for nonvolatile semiconductor memory, and enables large improvement in the speed of the semiconductor device that contains the usual transistor which does not have a memory and usual nonvolatile semiconductor memory.

[0175] Fig. 119 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention.

This memory cell consists of an n type MOS transistor. With the memory cell structure of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention, the gate electrode 3 is formed in the surface of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
A concavity is prepared in the ends of the gate electrode 3, and the charge accumulation layer 4 (4a, 4b) is formed in each concavity.
The oxide film 30 is formed between the charge accumulation layer 4 and the gate electrode 3.
The sidewall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9.
The electric conduction layer 12 is formed in each surface of the gate electrode 3 and n+ type diffusion layer 11.

[0176] The memory cell of the non-volatile memory concerning the 13th embodiment form of this invention has LDD structure which constituted the source field and the drain field from an n- type diffusion layer 10 of low impurity concentration, and an n+ type diffusion layer 11 of high impurity concentration. And the charge accumulation layer 4 (4a, 4b) is formed in the both ends of the gate electrode 3. An electron is accumulated to these two charge accumulation layers 4a and 4b.
The store status are four possibility

(1) Neither charge accumulation layer 4a nor 4b is accumulating the electron,
(2) only charge accumulation layer 4a is accumulating the electron, the status that only
(3) only charge accumulation layer 4b is accumulating the electron
(4) Both charge accumulation layers 4a and 4b are accumulating the electron.

The amount of the change of threshold potential produced by the existence of the electron held at these two charge accumulation layers 4a and 4b is made to correspond to a storage information "00", "01", "10", and "11."
Moreover, with this memory cell structure, since the charge accumulation layer 4 is located in the upper part of a channel field edge, the threshold voltage of a channel field center section is decided only by impurity concentration of a channel field, and it does not depend for it on the store status of the electron of the charge accumulation layer 4.
Therefore, the fault deletion (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and the poor leakage which originates in a fault deletion by that cause, a poor program, and poor read-out must have been produced.
Moreover, the leakage current between a source field and a drain field can be suppressed only by the gate voltage, and can realize highly reliable non-volatile memory.
What is necessary is for the charge accumulation layer 4 just to consist of a high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the membranous quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.
If the 1st gate insulator layer 13 is furthermore constituted from a silicon nitride (Si_3N_4 layer) which has the dielectric constant of an about 2 times of a silicon oxide (SiO_2 layer), a silicon-oxide conversion thickness can stabilized and the very thin gate insulator layer which is from about 4nm to 11nm can be realized.
For example, since the real thickness in 5nm of the silicon nitride whose silicon-oxide conversion thickness is about 10nm, the induction of the direct tunnel (DT) injection is not carried out.
Therefore, the voltage at the time of an electronic injection extraction operation is reduced in low-battery, and not only miniaturization of a memory cell but miniaturization of a circumference high-voltage operation element of it is attained.

[0177] Although n- type diffusion layer 10 is established for the purpose of the pressure-proof enhancement in a source field and a drain field and LDD structure is constituted from a memory

cell of the non-volatile memory concerning the 13th embodiment form of this invention, a source field and a drain field may consist of single drain structure and double drain structure.

[0178] Next, an operation of the non-volatile memory concerning the 13th embodiment form of this invention is explained using the Fig. 120 and the Fig. 121 . Fig. 120 is a cross section of the non-volatile memory explaining a write-in operation. Fig. 121 is a cross section of the non-volatile memory explaining a deletion operation.
The memory cell of the Fig. 120 and the Fig. 121 consists of an n type MOS transistor.
As shown in Fig. 120 , at the time of the writing of a memory cell, voltage of about 6-8V is impressed to gate G, voltage of about 4-5V is impressed to drain D, respectively, and source S is grounded.
Thus, a voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field by the channel thermo electron (CHE). What is necessary is just to replace with the above the voltage impressed to drain D and each source S, in pouring an electron into charge accumulation layer 4b by the side of a source field.
On the other hand, as shown in Fig. 121 , a deletion of a memory cell impresses a negative voltage (at least -5V) to gate G, and is performed by Fig. out an electron from the charge accumulation layers 4a and 4b using a Fowler Nordheimt (FN) type tunnel current.
Moreover, when two or more memory cells share gate G, an electron can be simultaneously drawn out from those memory cells. In this case, source S and drain D should just be taken as the p type semiconductor substrate 1 and this potential.
Moreover, it is also possible to impress the right voltage different from the potential of the p type semiconductor substrate 1 to a drain electrode, and to draw out an electron for a source electrode only from floating potential (Floating), then charge accumulation layer 4b by the side of a drain electrode.
What is necessary is to impress a right voltage to a source electrode, in drawing out an electron only from charge accumulation layer 4a by the side of a source electrode, and just to let a drain electrode be floating potential.

[0179] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current flowing between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0180] Next, the operation of the non-volatile memory concerning the 13th embodiment form of this invention which consists of a p type MOS transistor is explained using the Fig. 122 and the Fig. 123.
Fig. 122 is a cross section of the non-volatile memory explaining a write-in operation.
Fig. 123 is a cross section of the non-volatile memory explaining a deletion operation.
The memory cell of the Fig. 122 and the Fig. 123 consists of a p type MOS transistor.
As shown in Fig. 122, at the time of the writing of a memory cell, about 5V is impressed to gate G, and about -5V is impressed to drain D, respectively, and let source S be floating potential.
Thus, a voltage is impressed, energy is given the electron of the tunnel phenomenon reason between band-bands by the electric field near the drain field, and an electron is poured into charge accumulation layer 4b by the side of a drain field.
What is necessary is just to replace with the above the voltage impressed to drain D and each source S, in pouring an electron into charge accumulation layer 4a by the side of a source field.
On the other hand, as shown in Fig. 123 , a deletion of a memory cell is carried out by impressing a negative voltage (at least -5V) to gate G and drawing an electron from the charge accumulation layers 4a and 4b using FN current.

Moreover, when two or more memory cells share gate G, an electron can be simultaneously drawn out from those memory cells. In this case, source S and drain D are taken as the n-type-semiconductor substrate 19, this potential, or floating potential.

[0181] Moreover, although illustration is not carried out, read-out of a memory cell is performed by detecting the read-out current flowing between source S and drain D.
It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the store status of the charge accumulation layers 4a and 4b.
To which a bias shall be carried out between source S and drain D should just choose the direction where the modulation of current transfer characteristics appears notably.
According to four store status of the charge accumulation layers 4a and 4b, four different current transfer characteristics are obtained and, thereby, the information for 2 bits can be memorized in one cell.

[0182] In the 13th embodiment form of this invention, the usual MOS transistor as shown in Fig. 124, which does not have a memory, is also realizable.
Because, in this MOS transistor, the charge accumulation layer 4 is arranged only on the source drain field 10 and 11, and is not arranged on the channel field.
For this reason, the conduction property of this MOS transistor is because influence is not received in the hold status of the charge of the charge accumulation layer 4 at all.
Furthermore, by presence of the concavity of the gate electrode 3, the parasitic capacitance between gate-source drains is reduced and it also has the advantageous point that the fast turn around of an MOS transistor becomes possible.

[0183] (14th Embodiment Form) Next, the 14th embodiment form of this invention is explained.
The 14th embodiment form serves as the configuration of having made the charge accumulation layer 4 and the sidewall spacer 9 unifying, in the 13th embodiment form of the above.
Fig. 125 is a cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention.
This memory cell consists of an n type MOS transistor.
With the memory cell structure of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention, the gate electrode 3 is formed in the surface of the p type semiconductor substrate 1 through the 1st gate insulator layer 13.
A concavity is prepared in the ends of the gate electrode 3, and the charge accumulation layer 4 (4a, 4b) is formed in each concavity.
The oxide film 30 is formed between the charge accumulation layer 4 and the gate electrode 3.
The sidewall spacer 9 is formed in the side face of the gate electrode 3 through an oxide film 16, and a part of this sidewall spacer 9 constitutes the charge accumulation layer 4. n- type diffusion layer 10 of the low impurity concentration which touches a channel field, and n+ type diffusion layer 11 of the high impurity concentration located in the outside of this n- type diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of the sidewall spacer 9.
The electric conduction layer 12 is formed in each surface of gate electrode 3 and n+ type diffusion layer 11.

[0184] What is necessary is for the 14th embodiment form of this invention just to constitute the sidewall spacer 9 and the charge accumulation layer 4 from the high silicon nitride of the charge store capacity by CVD.
It is because the charge hold property of being hard to receive influence in the film quality of a lower insulator layer can be acquired by accumulating an electron to the dispersed charge trapping level of a silicon nitride.
Moreover, if constituted from a silicon layer and a polycrystal silicon layer, it can manufacture cheaply.

[0185] In the 14th embodiment form of this invention, a usual MOS transistor as shown in Fig.

126 is realizable as well as the 13th embodiment of the above

[0186]
[Effect of the Invention] According to this invention, the structure of the nonvolatile semiconductor memory, which can memorize the information for two or more bits by the easy cellular structure, is realizable.

[0187] According to this invention, the manufacture technique of the nonvolatile semiconductor memory which manufactures the nonvolatile semiconductor memory, which memorizes the information for two or more bits in an easy manufacture process, is realizable.

[0188] According to this invention, the structure of a semiconductor memory containing non-volatile memory capable of electrically writing/deleting and volatile memory capable of high-speed writing in and reading out, is realizable with a simple cell structure.

[0189] According to this invention, the manufacture technique of a semiconductor memory containing non-volatile memory capable of electrically writing/deleting and volatile memory capable of high-speed writing in/reading out, is realizable with simple manufacture process.

[Brief Description of the Drawings]
[Fig. 1] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 2] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 3] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 4] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 5] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 6] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 7] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 8] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 9] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 1st embodiment form of this invention.

[Fig. 10] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 11] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 12] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 13] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 14] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 15] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 16] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 17] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 18] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 19] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 2nd embodiment form of this invention.

[Fig. 20] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.

[Fig. 21] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.

[Fig. 22] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 4th embodiment form of this invention.

[Fig. 23] It is the cross section showing the structure of the MOS transistor which constitutes the circumference circuit of the non-volatile memory concerning the 5th embodiment form of this invention.

[Fig. 24] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 25] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 26] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 27] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 28] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 29] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 30] It is the cross section showing the manufacturing process of the MOS transistor of Fig. 23 .

[Fig. 31] It is the cross section showing the memory cell structure of the nonvolatile

semiconductor memory carried in the semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 32] It is the cross section showing the memory cell structure of the volatile semiconductor memory carried in the semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 33] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 34] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 35] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 36] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 37] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 38] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 39] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 40] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 41] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 42] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 43] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 44] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 45] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 46] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 47] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 48] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 49] It is the cross section showing the manufacturing process of the memory cell of the

volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 50] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 51] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 52] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 6th embodiment form of this invention.

[Fig. 53] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory carried in the semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 54] It is the cross section showing the memory cell structure of the volatile semiconductor memory carried in the semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 55] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 56] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 57] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 58] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 59] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 60] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 61] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 62] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 63] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 64] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 65] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 66] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 67] It is the cross section showing the manufacturing process of the memory cell of the

volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 68] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 69] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 70] It is the cross section showing the manufacturing process of the memory cell of the volatile semiconductor memory concerning the 7th embodiment form of this invention.

[Fig. 71] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 72] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 73] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 74] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 75] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 76] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 77] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 78] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 79] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 80] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 81] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 82] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 8th embodiment form of this invention.

[Fig. 83] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 84] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 85] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 86] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 87] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 88] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 89] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 9th embodiment form of this invention.

[Fig. 90] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 91] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 92] It is a cross section explaining an operation of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 93] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 94] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 95] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 96] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 97] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 98] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 99] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 100] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 101] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 10th embodiment form of this invention.

[Fig. 102] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 103] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 104] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 105] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 106] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 107] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 108] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 11th embodiment form of this invention.

[Fig. 109] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 110] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 111] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 112] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 113] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 114] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 115] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 116] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 117] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 118] It is the cross section showing the manufacturing process of the memory cell of the nonvolatile semiconductor memory concerning the 12th embodiment form of this invention.

[Fig. 119] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention.

[Fig. 120] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of an n type MOS transistor.

[Fig. 121] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of an n type MOS transistor.

[Fig. 122] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of a p type MOS

transistor.

[Fig. 123] It is a cross section explaining the operation of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention which consisted of a p type MOS transistor.

[Fig. 124] It is the cross section showing the structure of the MOS transistor which has the same gate structure as the memory cell of the nonvolatile semiconductor memory concerning the 13th embodiment form of this invention.

[Fig. 125] It is the cross section showing the memory cell structure of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention.

[Fig. 126] It is the cross section showing the structure of the MOS transistor which has the same gate structure as the memory cell of the nonvolatile semiconductor memory concerning the 14th embodiment form of this invention.

[Description of Notations]
1 P Type Semiconductor Substrate
2 Gate Insulator Layer
3 Gate Electrode (1st Gate Electrode)
4 Charge Accumulation Layer
5 1st Oxide Film
6 Nitride
7 2nd Oxide Film
8 2nd Gate Electrode
9 Sidewall Spacer
10 N- Type Diffusion Layer
11 N+ Type Diffusion Layer
12 Electric Conduction Layer
13 1st Gate Insulator Layer
14 2nd Gate Insulator Layer
15 3rd Gate Insulator Layer
16 Oxide Film
17 Space for Charge Accumulation Layer Formation
18 Silicon Nitride
19 N-type-Semiconductor Substrate
20 P- Type Diffusion Layer
21 P+ Type Diffusion Layer
22, 27 Photoresist (photoresist pattern)
23 Tunnel Insulator Layer
24 4th Gate Insulator Layer
25 Channel Field
26 Level Difference
28 Polycrystal Silicon Layer

PATENT ABSTRACTS OF JAPAN

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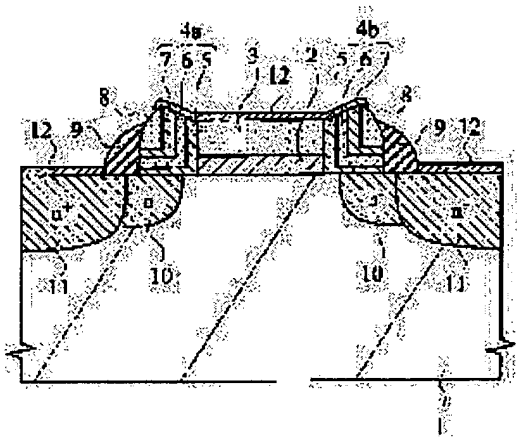
(54) SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR MANUFACTURING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nonvolatile semiconductor storage device for storing information for plural bits, using a simple cell structure.
SOLUTION: In this new structure of a nonvolatile semiconductor storage device for storing information for plural bits, the edge part of a gate electrode is provided with a charge-storing layer 4 for storing electrons. Thus, information on plural bits can be stored by storing the electrons in the charge storage layer 4.



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CLAIMS

[Claim(s)]
[Claim 1] A non-volatile semiconductor memory characterized by providing the following. The 1st gate electrode arranged through a gate insulator layer on a principal plane of a semiconductor substrate this -- a charge accumulation layer arranged on the side of the 1st gate electrode The 2nd gate electrode arranged through said charge accumulation layer on the side of said 1st gate electrode A conductive layer which connects electrically said 1st gate electrode and said 2nd gate electrode
[Claim 2] A manufacture method of a non-volatile semiconductor memory characterized by to include at least a process which forms a conductive layer which connects electrically a process which forms the 1st gate electrode through a gate insulator layer on a principal plane of a semiconductor substrate, a process which carries out sequential formation of a charge accumulation layer and the 2nd gate electrode on the side of said 1st gate electrode, and said 1st gate electrode and said 2nd gate electrode.
[Claim 3] A non-volatile semiconductor memory characterized by having a gate insulator layer which has been arranged on a principal plane of a semiconductor substrate, and which consists of the 1st, 2nd, and 3rd insulator layers, a charge accumulation layer arranged at the edge of said 2nd insulator layer, and a gate electrode arranged on said gate insulator layer.
[Claim 4] A process which forms a gate insulator layer which carries out sequential formation of the 1st, 2nd, and 3rd insulator layers, and consists of these 1st, 2nd, and 3rd insulator layers on a principal plane of a semiconductor substrate, After depositing a gate electrode component on the upper part of this gate insulator layer, this gate electrode component and a gate insulator layer by carrying out patterning A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms a gate electrode, a process which removes an edge of said 2nd insulator layer selectively, and forms space, and a process which forms a charge accumulation layer in this space [Claim 5] A semiconductor memory characterized by providing the following. the 1st lower insulator layer arranged on a principal plane of a semiconductor substrate -- this -- the 1st medium insulator layer arranged in the upper part of a center of the 1st lower insulator layer -- the 1st up insulator layer arranged in the upper part of the 1st charge accumulation layer arranged in the upper part of an edge of said 1st lower insulator layer, said 1st medium insulator layer, and the 1st charge accumulation layer -- and -- this -- a non-volatile semiconductor memory which has the 1st gate electrode arranged in the upper part of the 1st up insulator layer The 2nd lower insulator layer which has been arranged on a principal plane of said semiconductor substrate and which consists of the same material as said 1st medium insulator layer, a principal plane top of said semiconductor substrate -- and -- this -- an ultra-thin insulator layer arranged to ends of the 2nd lower insulator layer -- The 2nd charge accumulation layer which has been arranged in the upper part of this ultra-thin insulator layer and which consists of the same material as said 1st charge accumulation layer, the 2nd up insulator layer which consists of the same material as said 1st up insulator layer arranged in the upper part of said 2nd lower insulator layer and the 2nd charge accumulation layer -- and -- this -- an volatile semiconductor memory which has the 2nd gate electrode arranged in the upper part of the 2nd up insulator layer
[Claim 6] A semiconductor memory characterized by providing the following. the 1st lower insulator layer arranged on a principal plane of a semiconductor substrate -- this -- the 1st medium insulator layer arranged in the upper part of a center of the 1st lower insulator layer -- the 1st up insulator layer arranged in the upper part of the 1st charge accumulation layer arranged in the upper part of an edge of said 1st lower insulator layer, said 1st medium insulator layer, and the 1st charge accumulation layer -- this -- a non-volatile semiconductor memory which has the 1st gate electrode arranged in the upper part of the 1st up insulator layer the 2nd charge accumulation layer which consists of the same material as said 1st charge accumulation layer arranged on an ultra-thin insulator layer arranged on a principal plane of said semiconductor substrate, and this ultra-thin insulator layer -- this -- the 2nd up insulator layer arranged on the 2nd charge accumulation layer -- this -- an volatile semiconductor memory which has the 2nd gate electrode

arranged on the 2nd up insulator layer
[Claim 7] a lower insulator layer [which has been arranged on a principal plane of a semiconductor substrate], and principal plane top of said semiconductor substrate -- and the volatile semiconductor memory characterized by to have an up insulator layer arranged in the upper part of an ultra-thin insulator layer arranged to ends of this lower insulator layer, a charge accumulation layer arranged in the upper part of this ultra-thin insulator layer, and a said lower insulator layer and a charge accumulation layer, and a gate electrode arranged in the upper part of this up insulator layer.
[Claim 8] An volatile semiconductor memory characterized by having an ultra-thin insulator layer arranged on a principal plane of a semiconductor substrate, a charge accumulation layer arranged on this ultra-thin insulator layer, an insulator layer arranged on this charge accumulation layer, and a gate electrode arranged on this insulator layer.
[Claim 9] A process which forms the 1st insulator layer in a part on a principal plane of a semiconductor substrate, the upper part of this 1st insulator layer, and a principal plane of said semiconductor substrate a part A process which carries out sequential formation of the 2nd and 3rd insulator layers except, By process which deposits a gate electrode component on the upper part of this 3rd insulator layer, and carrying out patterning of this gate electrode component, said 3rd insulator layer, said 2nd insulator layer, and the 1st insulator layer By process which forms the 1st gate electrode, and carrying out patterning of said gate electrode component, said 3rd insulator layer, and the 2nd insulator layer a process which forms the 2nd gate electrode -- this -- a manufacture method of a semiconductor memory characterized by including at least a process which removes selectively an edge of the 2nd insulator layer of both 1st and 2nd gate electrodes, and forms space, and a process which forms a charge accumulation layer in this space.
[Claim 10] A process which carries out sequential formation of the 1st, 2nd, and 3rd insulator layers on a principal plane of a semiconductor substrate characterized by providing the following, a process which forms the 1st gate electrode by carrying out patterning of this gate electrode component, said 3rd insulator layer, said 2nd insulator layer, and the 1st insulator layer after depositing the 1st gate electrode component on the upper part of this 3rd insulator layer -- this -- the 1st gate electrode formation process, simultaneously a process performed A process which forms the 2nd gate electrode formation field in a part of principal plane of said semiconductor substrate by removing said gate electrode component, said 3rd insulator layer, said 2nd insulator layer, and the 1st insulator layer A process which removes selectively an edge of the 2nd insulator layer of said 1st gate electrode, and forms space A process which forms an ultra-thin insulator layer on a principal plane of said semiconductor substrate After depositing a material which constitutes a charge accumulation layer on a principal plane of said semiconductor substrate, this charge accumulation layer component by carrying out anisotropic etching On a process which forms a charge accumulation layer in space of said 1st gate electrode, and a principal plane of said semiconductor substrate after depositing the 4th insulator layer and the 2nd gate electrode component -- this -- a process which forms the 2nd gate electrode by carrying out patterning of the 2nd gate electrode component, said 4th insulator layer, said charge accumulation layer component, and ultra-thin insulator layer
[Claim 11] A non-volatile semiconductor memory characterized by having a gate insulator layer which has been arranged on a principal plane of said semiconductor substrate containing heights arranged on a principal plane of a semiconductor substrate, and these heights, and which consists of the 1st, 2nd, and 3rd insulator layers, a charge accumulation layer arranged at the edge of said 2nd insulator layer, and a gate electrode arranged on said gate insulator layer.
[Claim 12] A process which forms a gate insulator layer which carries out sequential formation of the 1st, 2nd, and 3rd insulator layers, and consists of these 1st, 2nd, and 3rd insulator layers on a principal plane of a process which forms heights on a principal plane of a semiconductor substrate, and said semiconductor substrate containing these heights, After depositing a gate electrode component on the upper part of this gate insulator layer, this gate electrode component and a gate insulator layer by carrying out patterning A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms a gate electrode, a process which removes an edge of said 2nd insulator layer selectively, and forms space, and a process which forms a charge accumulation layer in this space.
[Claim 13] A non-volatile semiconductor memory characterized by having a gate insulator layer which has been arranged on a principal plane of said semiconductor substrate containing heights arranged on a principal plane of a semiconductor substrate, and these heights, and which consists of the 1st and 2nd insulator layers, a charge accumulation layer arranged between these 1st and 2nd insulator layers, and a gate electrode arranged on said gate insulator layer.
[Claim 14] A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms heights on a principal plane of a semiconductor substrate, a process which carries out sequential formation of the 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer on a principal plane of said semiconductor substrate containing these heights, and a process which forms a gate electrode by carrying out patterning of this 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer.

[Claim 15] A non-volatile semiconductor memory characterized by having a gate insulator layer which has been arranged on a principal plane of said semiconductor substrate including a crevice arranged on a principal plane of a semiconductor substrate, and this crevice, and which consists of the 1st, 2nd, and 3rd insulator layers, a charge accumulation layer arranged at the edge of said 2nd insulator layer, and a gate electrode arranged on said gate insulator layer.
[Claim 16] A process which forms a gate insulator layer which carries out sequential formation of the 1st, 2nd, and 3rd insulator layers, and consists of these 1st, 2nd, and 3rd insulator layers on a principal plane of a process which forms a crevice on a principal plane of a semiconductor substrate, and said semiconductor substrate including this crevice, After depositing a gate electrode component on the upper part of this gate insulator layer, this gate electrode component and a gate insulator layer by carrying out patterning A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms a gate electrode, a process which removes an edge of said 2nd insulator layer selectively, and forms space, and a process which forms a charge accumulation layer in this space.
[Claim 17] A non-volatile semiconductor memory characterized by having a gate insulator layer which has been arranged on a principal plane of said semiconductor substrate including a crevice arranged on a principal plane of a semiconductor substrate, and this crevice, and which consists of the 1st and 2nd insulator layers, a charge accumulation layer arranged between these 1st and 2nd insulator layers, and a gate electrode arranged on said gate insulator layer.
[Claim 18] A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms a crevice on a principal plane of a semiconductor substrate, a process which carries out sequential formation of the 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer on a principal plane of said semiconductor substrate containing these heights, and a process which forms a gate electrode by carrying out patterning of this 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer.
[Claim 19] A process which forms a gate insulator layer which carries out sequential formation of the 1st, 2nd, and 3rd insulator layers, and consists of these 1st, 2nd, and 3rd insulator layers on a principal plane of a process which forms a crevice on a principal plane of a semiconductor substrate, and said semiconductor substrate including this crevice, After depositing a gate electrode component on the upper part of this gate insulator layer, this gate electrode component by removing by chemical mechanical polishing method A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms a gate electrode embedded in said crevice, a process which removes an edge of said 2nd insulator layer selectively, and forms space, and a process which forms a charge accumulation layer in this space.
[Claim 20] A process which forms a crevice on a principal plane of a semiconductor substrate, and a process which carries out sequential formation of the 1st insulator layer, a charge accumulation layer component, and the 3rd insulator layer on a principal plane of said semiconductor substrate including this crevice, A manufacture method of a non-volatile semiconductor memory characterized by including at least a process which forms a gate electrode embedded in said crevice by removing this gate electrode component by chemical mechanical polishing method after depositing a gate electrode component on the upper part of this 3rd insulator layer.
[Claim 21] A non-volatile semiconductor memory characterized by having a gate electrode arranged through a gate insulator layer on a principal plane of a semiconductor substrate, a crevice arranged at the edge of this gate electrode, and a charge accumulation layer arranged through an insulator layer in this crevice at the upper part of both a channel field and a source drain field.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the semiconductor memory which wrote in electrically, wrote in an eliminable non-volatile semiconductor memory and its manufacture method, and a high speed, and loaded together the volatile semiconductor memory which can be read, its manufacture method and the non-volatile semiconductor memory, and the volatile semiconductor memory on the same chip, and its manufacture method.
[0002]
[Description of the Prior Art] By nonvolatile memory, such as the conventional EEPROM (Electrically Erasable and Programmable Read Only Memory), the information for 1 bit is memorized in one cel by realizing two thresholds which are different in one cel. On the other hand, for memory densification, four or more thresholds are given to one cel, and the technology of memorizing the above information in one cel by 2 bits is proposed (M.Bauer et al., ISSCC95, p.132). However, in order to realize this technology, the charge maintenance reliability more than before is required of exact control of threshold voltage, the exact detection for a small change of threshold voltage, and a pan. Therefore, with this technology, the engine performance equivalent to the former cannot actual necessarily be obtained. Moreover, this technology also has the problem that the manufacture yield is low. For this reason, the cellular structure which memorizes the information for two or more bits by accumulating a charge in two or more physically different locations is newly proposed (B.Eitan et al, IEDM96, p169, Fig6). Moreover, the structure of establishing a charge accumulation layer in the side attachment wall of a gate electrode is proposed by this invention person as the cellular structure of resemblance in it before (United States Patent number No. 4881108). However, the manufacturing process of these cellular structures is very complicated, and has the problem that the controllability of a channel field is not enough, either.
[0003] The need of writing in electrically from the demand of the system-on-chip of these days on the other hand, writing in eliminable nonvolatile memory and an eliminable high speed, and realizing volatile memory which can be read on the same chip is increasing. The demand of the nonvolatile memory which has floating-gate structures, such as EEPROM and a flash memory, especially, and VLSI consolidated with the dynamic RAM in which high-speed operation is possible is increasing rapidly. However, the memory cell of a dynamic RAM in recent years is becoming the very complicated three-dimensional structures, such as trench structure and stack structure. For this reason, if it is going to load together floating-gate mold nonvolatile memory and a dynamic RAM, from the difference in that memory cell structure, a manufacture process will be complicated and a mask routing counter will also increase. Therefore, the manufacturing cost of the mixed-loading chip will become very big.
[0004] If the memory cell of a dynamic RAM is realized using the memory cell structure of the nonvolatile memory of a floating-gate mold, it is possible for a manufacture process to be simplified by communalization of the cellular structure and to reduce a manufacturing cost by it. However, it is difficult to realize the high-speed writing which is the feature of a dynamic RAM in the communalized memory cell.
[0005]
[Problem(s) to be Solved by the Invention] This invention is accomplished in view of the above-mentioned situation, and aims at offering the structure of a non-volatile semiconductor memory where the information for two or more bits is memorizable by the easy cellular structure.
[0006] Other objects of this invention are offering the manufacture method of a non-volatile semiconductor memory of manufacturing the non-volatile semiconductor memory which memorizes the information for two or more bits in an easy manufacture process.
[0007] The object of further others of this invention is offering the structure of the semiconductor memory which wrote

in electrically by the easy cellular structure and loaded together eliminable nonvolatile memory and the volatile memory in which read-out write-in [high-speed] is possible.
[0008] The object of further others of this invention is offering the manufacture method of the semiconductor memory which wrote in electrically in the easy manufacture process and loaded together eliminable nonvolatile memory and the volatile memory in which read-out write-in [high-speed] is possible.
[0009]
[Means for Solving the Problem] In order to attain the above-mentioned object, the 1st feature of this invention The 1st gate electrode arranged through a gate insulator layer on a principal plane of a semiconductor substrate, A charge accumulation layer is minded on a charge accumulation layer arranged on the side of the 1st gate electrode, and the side of the 1st gate electrode. It is the non-volatile semiconductor memory which possesses a conductive layer which connects electrically the 2nd arranged gate electrode, and the 1st gate electrode and the 2nd gate electrode at least.
[0010] The 2nd feature of this invention is the non-volatile semiconductor memory which possesses at least a gate insulator layer which has been arranged on a principal plane of a semiconductor substrate, and which consists of the 1st, 2nd, and 3rd insulator layers, a charge accumulation layer arranged at the edge of the 2nd insulator layer, and a gate electrode arranged on a gate insulator layer.
[0011] The 3rd feature of this invention is a semiconductor memory consolidated with a non-volatile semiconductor memory and an volatile semiconductor memory. A non-volatile semiconductor memory The 1st lower insulator layer arranged on a principal plane of a semiconductor substrate, and the 1st medium insulator layer arranged in the upper part of a center of the 1st lower insulator layer, The 1st up insulator layer arranged in the upper part of the 1st charge accumulation layer arranged in the upper part of an edge of the 1st lower insulator layer, and the 1st medium insulator layer and the 1st charge accumulation layer, The 1st gate electrode arranged in the upper part of the 1st up insulator layer is provided at least. An volatile semiconductor memory The 1st medium insulator layer and the 2nd lower insulator layer which consists of the same material arranged on a principal plane of a semiconductor substrate, On a principal plane of a semiconductor substrate, and an ultra-thin insulator layer arranged to ends of the 2nd lower insulator layer, The 1st charge accumulation layer and the 2nd charge accumulation layer which consists of the same material arranged in the upper part of an ultra-thin insulator layer, The 2nd gate electrode arranged in the upper part of the 1st up insulator layer and the 2nd up insulator layer which consists of the same material arranged in the upper part of the 2nd lower insulator layer and the 2nd charge accumulation layer, and the 2nd up insulator layer is provided at least.
[0012] The 4th feature of this invention is a semiconductor memory consolidated with a non-volatile semiconductor memory and an volatile semiconductor memory. A non-volatile semiconductor memory The 1st lower insulator layer arranged on a principal plane of a semiconductor substrate, and the 1st medium insulator layer arranged in the upper part of a center of the 1st lower insulator layer, The 1st up insulator layer arranged in the upper part of the 1st charge accumulation layer arranged in the upper part of an edge of the 1st lower insulator layer, and the 1st medium insulator layer and the 1st charge accumulation layer, The 1st gate electrode arranged in the upper part of the 1st up insulator layer is provided at least. An volatile semiconductor memory The 1st charge accumulation layer and the 2nd charge accumulation layer which consists of the same material arranged on an ultra-thin insulator layer arranged on a principal plane of a semiconductor substrate, and an ultra-thin insulator layer, The 2nd gate electrode arranged on the 2nd up insulator layer arranged on the 2nd charge accumulation layer and the 2nd up insulator layer is provided at least.
[0013] The 5th feature of this invention is the non-volatile semiconductor memory which possesses at least a gate insulator layer which has been arranged on a principal plane of a semiconductor substrate including heights or a crevice arranged on a principal plane of a semiconductor substrate, and heights or a crevice, and which consists of the 1st, 2nd, and 3rd insulator layers, a charge accumulation layer arranged at the edge of the 2nd insulator layer, and a gate electrode arranged on a gate insulator layer.
[0014] The 6th feature of this invention is the non-volatile semiconductor memory which possesses at least a gate insulator layer which has been arranged on a principal plane of a semiconductor substrate including heights or a crevice arranged on a principal plane of a semiconductor substrate, and heights or a crevice, and which consists of the 1st and 2nd insulator layers, a charge accumulation layer arranged between the 1st and 2nd insulator layers, and a gate electrode arranged on a gate insulator layer.
[0015] ** is provided for a charge accumulation layer arranged through an insulator layer in a gate electrode with which the 7th feature of this invention has been arranged through a gate insulator layer on a principal plane of a semiconductor substrate, a crevice arranged at the edge of a gate electrode, and a crevice at least, and it is the non-volatile semiconductor memory with which a charge accumulation layer is arranged in the upper part of both a channel field and a source drain field.
[0016]

[Embodiment of the Invention] With reference to a drawing, the gestalt of operation of this invention is explained below. In the publication of the following drawings, the sign of identically the same into a similar portion or resemblance is attached. However, a drawing is typical and it should care about that the ratio of the relation between thickness and a flat-surface size and the thickness of each class etc. differs from an actual thing. Therefore, concrete thickness and a concrete size should be judged in consideration of the following explanation. Moreover, of course, the portion from which the relation and the ratio of a mutual size differ also in between drawings is contained.
[0017] (Gestalt of the 1st operation) Drawing 1 is the cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 1st of this invention. This memory cell consists of n mold MOS transistors. With the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 1st of this invention, the 1st gate electrode 3 is formed in the front face of the p type semiconductor substrate 1 through the gate insulator layer 2, and the charge accumulation layer 4 (4a, 4b) is established in the both-sides side of the 1st gate electrode 3. This charge accumulation layer 4 has the laminated structure, the 1st oxide film 5 and the 2nd layer consist of nitrides 6, and the 3rd layer consists of the 2nd oxide film 7 for the 1st layer. Furthermore, the 2nd gate electrode 8 is formed in the upper part of the charge accumulation layer 4. The sidewall spacer 9 is formed in the side of the charge accumulation layer 4, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9. the 1st gate electrode 3, the charge accumulation layer 4, the 2nd gate electrode 8, and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face. The 1st gate electrode 3 and the 2nd gate electrode 8 are electrically connected through this conductive layer 12.
[0018] The memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 1st of this invention has the LDD (Lightly doped drain) structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And the charge accumulation layer 4 is formed in the both-sides side of the 1st gate electrode 3, and a changed part of the threshold voltage produced by the existence of the electron held at the nitride 6 of these two charge accumulation layers 4 is made to correspond to "00" of storage information, "01", "10", and "11." Furthermore, the 2nd gate electrode 8 is formed in the upper part of the charge accumulation layer 4, by carrying out electrical installation of this 2nd gate electrode 8 to the 1st gate electrode 3, the controllability of a channel field is raised and detection for threshold voltage change is made easy.
[0019] Next, actuation of the nonvolatile memory concerning the gestalt of operation of the 1st of this invention is explained using drawing 2 thru/or drawing 4 . Drawing 2 is the cross section of the nonvolatile memory explaining write-in actuation. Drawing 3 is the cross section of the nonvolatile memory explaining read-out actuation. Drawing 4 is the cross section of the nonvolatile memory explaining elimination actuation. As shown in drawing 2 , at the time of the writing of a memory cell, high tension (- 10 V) is impressed to Gate G, and the source S which applies high tension (- 8 V) to the drain D close to charge accumulation layer 4b which accumulates an electron simultaneously, and does not approach is grounded. Thus, if voltage is impressed, a channel thermoelectron (Channel Hot Electron) will be generated and this thermoelectron will be captured by the nitride 6 of charge accumulation layer 4b. Charge accumulation layer 4b's capture of an electron changes the threshold voltage of a cel transistor. Read-out of a memory cell is performed by detecting a changed part of threshold voltage. As shown in drawing 3 , voltage 5V are added to Gate G, voltage 3V are simultaneously impressed to Drain D, and, specifically, the difference of the amount of current is detected with a sense amplifier. Moreover, as shown in drawing 4 , elimination of a memory cell impresses positive voltage (- 9 V) to the drain D which impresses negative voltage (- -6 V) to Gate G, and approaches charge accumulation layer 4b eliminated, and is performed by emitting trapped electron to charge accumulation layer 4b. In addition, Source S and Drain D of an MOS transistor can be done in the symmetry as everyone knows, and, generally it is possible to replace Source S and Drain D. Therefore, also in the above-mentioned explanation, it is possible to replace Drain D with Source S.
[0020] Next, the manufacture method of the memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 1st of this invention is explained using drawing 5 thru/or drawing 9 . As first shown in drawing 5 , the 25nm gate insulator layer 2 is formed by thermal oxidation on the p type semiconductor substrate 1. then, the p type semiconductor substrate 1 whole surface -- LPCVD (Low Pressure Chemical Vapor Deposition) -- after depositing the 300nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with well-known exposure technology and etching technology, and the 1st gate electrode 3 is formed.
[0021] Next, as shown in drawing 6 , after removing the gate insulator layer 2 of the front face of the p type semiconductor substrate 1 of the field which forms a source field and a drain field, the p type semiconductor substrate 1 is oxidized thermally in a 900 degrees C - 1200 degrees C oxidizing atmosphere, and the 1st 10nm oxide film 5 is

formed. and the 1st oxide-film 5 top -- LPCVD -- the 10nm - 100nm nitride 6 is deposited by law, and the 2nd about 5nm oxide film 7 is formed in nitride 6 front face with 900-degree C hydrogen burning oxidation or a CVD method after that.

[0022] next, it is shown in drawing 7 -- as -- the 2nd oxide-film 7 top -- for example, LPCVD -- RIE (Reactive Ion Etching) after depositing about 25-250nm polycrystalline silicon by law -- anisotropic etching by law is performed and the charge accumulation layer 4 which has the 2nd gate electrode 8 in the upper part is formed in the 1st gate electrode side by removing this polycrystalline silicon film, the 1st oxide film 5, a nitride 6, and the 2nd oxide film 7 by those thickness.

[0023] Next, as shown in drawing 8 , n-mold diffusion layer 10 of low high impurity concentration is formed. It is formed by activating the impurity which n-mold diffusion layer 10 used the 1st gate electrode 3 and the charge accumulation layer 4 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.

[0024] Next, as shown in drawing 9 , after forming the sidewall spacer 9 in the side attachment wall of the charge accumulation layer 4, n+ mold diffusion layer 11 of high high impurity concentration is formed. It is formed by activating the impurity which n+ mold diffusion layer 11 used the 1st gate electrode 3, the charge accumulation layer 4, and the sidewall spacer 9 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.

[0025] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere -- the 1st gate electrode 3, the charge accumulation layer 4, the 2nd gate electrode 8, and n+ mold diffusion layer 11 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. At this time, the thickness of the 1st oxide film 5, a nitride 6, the 2nd oxide film 7, especially a nitride 6 needs to be set up so that the refractory metal silicide layer on the 1st gate electrode 3 and the 2nd gate electrode 8 may carry out bridging. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 1 will be completed.

[0026] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 1 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.

[0027] According to the gestalt of operation of the 1st of this invention, since the 2nd gate electrode 8 was formed also in the upper part of the charge accumulation layer 4, the controllability of threshold voltage improves. In addition, although the gestalt of operation of the 1st of this invention explained the case where a memory cell was constituted from an n mold MOS transistor, the same effect is acquired even if it is the case where it constitutes from a p mold MOS transistor. Moreover, although the memory cell has LDD structure, they may be single drain structure and double drain structure.

[0028] (Gestalt of the 2nd operation) Next, the gestalt of operation of the 2nd of this invention is explained. Drawing 10 is the cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 2nd of this invention. This memory cell consists of n mold MOS transistors. With the memory cell structure of the nonvolatile memory concerning the gestalt of operation of the 2nd of this invention, the 2nd gate insulator layer 14 is formed in the front face of the p type semiconductor substrate 1 through the 1st gate insulator layer 13. And the charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14. On the 2nd gate insulator layer 14 and charge accumulation layer 4a, and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.

[0029] The memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 2nd of this invention has the LDD structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And it consists of three-layer cascade screens which a gate insulator layer turns into from the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer), and the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14. An electron is accumulated in these two charge accumulation layers 4a and 4b. That are recording condition (1) charge accumulation

layer 4a, All of 4b can take the condition which is not accumulating the electron, the condition that only (2) charge accumulation layer 4a is accumulating the electron, the condition that only (3) charge accumulation layer 4b is accumulating the electron, and four conditions of condition ** that (4) charge accumulation layers 4a and 4b are accumulating the electron. A changed part of the threshold voltage produced by the existence of the electron held in these two charge accumulation layers 4a and 4b is made to correspond to "00" of storage information, "01", "10", and "11." Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located above the channel field edge, the threshold voltage of a channel field center section is decided only by high impurity concentration of a channel field, and they do not depend for it on the are recording condition of the electron of the charge accumulation layers 4a and 4b. Therefore, fault elimination (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and cannot produce the poor leak which originates in fault elimination by that cause, a poor program, and poor read-out. Moreover, the leakage current between a source field and a drain field can be controlled only with gate voltage, and can realize highly reliable non-volatile semiconductor memory. What is necessary is for the charge accumulation layers 4a and 4b just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm, induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0030] Although n-mold diffusion layer 10 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 2nd of this invention, a source field and a drain field may consist of single drain structure and double drain structure. Although the 2nd gate insulator layer 14 prevents leak between charge accumulation layer 4a-4b, it can consist of silicon oxide, for example. Moreover, if the metal oxide film which has a high dielectric constant is used for the 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved. As a metal oxide film, there are TiO2, Ta 2O5, aluminum2O5, and PZT and SBT.

[0031] Next, actuation of the nonvolatile memory concerning the gestalt of operation of the 2nd of this invention is explained using drawing 11 and drawing 12 . Drawing 11 is the cross section of the nonvolatile memory explaining write-in actuation. Drawing 12 is the cross section of the nonvolatile memory explaining elimination actuation. As shown in drawing 11 , at the time of the writing of a memory cell, about 7-8V is impressed to Gate G, about 5V is impressed to Drain D, respectively, and Source S is grounded. Thus, voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field with a channel thermoelectron (CHE). the case where an electron is poured into charge accumulation layer 4a by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above-mentioned case On the other hand, as shown in drawing 12 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using Fowler Nordheim (FN) mold tunnel current. Moreover, when the gate electrode 3 is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, what is necessary is just to let Source S and Drain D be the p type semiconductor substrate 1 and this potential. Moreover, it is also possible to impress different positive voltage from the potential of the p type semiconductor substrate 1 to Drain D, and to draw out an electron for Source S only from charge accumulation layer 4a by the side of floating potential (Floating), then Drain D. What is necessary is to impress positive voltage to Source S, in drawing out an electron only from charge accumulation layer 4b by the side of Source S, and just to let Drain D be floating potential.

[0032] The writing of a memory cell can also be performed like elimination of a memory cell using FN current. About 10V is impressed between Gate G and the p type semiconductor substrate 1, and an electron is poured into the charge accumulation layers 4a and 4b with FN current. In this case, an electron can be simultaneously injected into two or more memory cells in which Gate G is common.

[0033] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the

charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0034] Next, the manufacture method of the memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 2nd of this invention is explained using drawing 13 thru/or drawing 19 . As first shown in drawing 13 , the small silicon nitride of charge storage capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. deposition of the small silicon nitride of charge storage capacity -- for example, JVD (Jet-Vapor-Deposition) -- it carries out by law. JVD -- law is indicated by reference "T.P.Ma, IEEE Transactions on Electron Devices, Volume 45 Number 3, and March 1998p680." Silicon oxide is deposited with a CVD method after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0035] next, it is shown in drawing 14 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, dry etching of the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask is carried out in self align.

[0036] Next, as shown in drawing 15 , the space 17 for charge accumulation layer formation is formed. This space 17 is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 2nd of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. Moreover, the space 17 for charge accumulation layer formation may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.

[0037] next, it is shown in drawing 16 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- it deposits so that the space 17 for charge accumulation layer formation may be thoroughly embedded by law in the high silicon nitride 18 of charge storage capacity. And as shown in drawing 17 , anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of high silicon nitrides of charge storage capacity are formed.

[0038] Next, as shown in drawing 18 , after forming an oxide film 16 all over p type semiconductor substrate 1, n-mold diffusion layer 10 of low high impurity concentration is formed. It forms by activating the impurity which n-mold diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.

[0039] Next, as shown in drawing 19 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, n+ mold diffusion layer 11 of high high impurity concentration is formed. It forms by activating the impurity which n+ mold diffusion layer 11 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.

[0040] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere -- the gate electrode 3 and n+ mold diffusion layer 11 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 10 will be completed.

[0041] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 10 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.

[0042] Thus, with the gestalt of the 2nd operation of this invention, the charge accumulation layers 4a and 4b can be formed in the lower part of the ends of the gate electrode 3 in self align. Therefore, detailed-ization of the direction of gate length of a cel transistor is attained. Thereby, large capacity and the non-volatile semiconductor memory of high density can be offered. Moreover, the cel area per bit is mostly reduced by half compared with the former, and non-

volatile semiconductor memory reduced substantially can be realized.
[0043] Moreover, the width of face of the direction of channel length of the charge accumulation layers 4a and 4b is easily controllable by accommodation of the etching speed difference of the 1st gate insulator layer 13 and the 3rd gate insulator layer 15, and the 2nd gate insulator layer 14, and etching time. Thereby, the charge accumulation layers 4a and 4b can be arranged to the symmetry. And since the charge accumulation layers 4a and 4b are electrically separated thoroughly by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b does not happen. Furthermore, since it is thoroughly insulated from a source field, a drain field, the gate electrode 3, and a channel field with the 1st insulator layer 13, 3rd insulator layer 15, and oxide film 16, the charge accumulation layers 4a and 4b can offer the non-volatile semiconductor memory which was excellent in the charge maintenance property. It is extended and formed in the direction of a channel field from the edge of the gate electrode 3, and the charge accumulation layers 4a and 4b are current transfer-characteristics ********** of a memory cell by the charge storage condition of the portion by the side of the channel field of the charge accumulation layers 4a and 4b. Therefore, if the gate length lay length of this portion is reduced to a limit, more detailed non-volatile semiconductor memory can be offered.
[0044] Furthermore, since the cellular structure is easily realizable at the usual CMOS process, non-volatile semiconductor memory can be manufactured by low cost using the existing production line.
[0045] (Gestalt of the 3rd operation) Next, the gestalt of operation of the 3rd of this invention is explained. In the gestalt of the 2nd operation shown in drawing 10 , silicon oxide and the 2nd gate insulator layer 14 are transposed to a silicon nitride, and the gestalt of operation of the 3rd of this invention transposes the 3rd gate insulator layer 15 for the 1st gate insulator layer 13 to silicon oxide. Hereafter, the manufacture method of the memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 3rd of this invention is explained with reference to drawing 13 thru/or drawing 15 .
[0046] First, the memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 3rd of this invention oxidizes thermally the p type semiconductor substrate 1, and forms the 1st gate insulator layer 13 which consists of about 10nm silicon oxide. after 1st gate insulator layer 13 formation and JVD -- the low silicon nitride of the charge storage capacity by law is deposited, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, silicon oxide is deposited with a CVD method and the about 10nm 3rd gate insulator layer 15 is formed (refer to drawing 13).
[0047] next, the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Dry etching of the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask continuously is carried out in self align (refer to drawing 14).
[0048] Next, the p type semiconductor substrate 1 is oxidized thermally, and thin silicon oxide is formed all over p type semiconductor substrate 1. Then, the space 17 for charge accumulation layer formation is formed. The space 17 for this charge accumulation layer formation is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. What is necessary is just to use for example, a phosphoric-acid system as an etching reagent with the gestalt of operation of the 3rd of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from silicon oxide and the 2nd gate insulator layer 14 is constituted from a silicon nitride. In addition, since the silicon nitride 14 hardly oxidizes depending on thermal oxidation processing, an oxide film is not formed in the side of the 2nd gate insulator layer, but, for this reason, its selectivity of etching improves (refer to drawing 15). Moreover, the space 17 for charge accumulation layer formation may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains CF4 gas. The subsequent process is the same as the gestalt of the 2nd operation.
[0049] (Gestalt of the 4th operation) Next, the gestalt of operation of the 4th of this invention is explained. Drawing 20 is the cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 4th of this invention. The gestalt of operation of the 4th of this invention is the example which constituted the memory cell from a p mold MOS transistor. As shown in drawing 20 , with the memory cell structure of the nonvolatile memory concerning the gestalt of operation of the 4th of this invention, the 2nd gate insulator layer 14 is formed in the front face of the n-type-semiconductor substrate 19 through the 1st gate insulator layer 13. And the charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14. On the 2nd gate insulator layer 14 and charge accumulation layer 4a, and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15. The

sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and p-mold diffusion layer 20 of the low high impurity concentration which touches a channel field, and p+ mold diffusion layer 21 of the high high impurity concentration located in the outside of this p-mold diffusion layer 20 are formed in the n-type-semiconductor substrate 19 of the lower part of this sidewall spacer 9. the gate electrode 3 and p+ mold diffusion layer 21 -- a conductive layer 12 is formed in each front face.

[0050] Next, actuation of the nonvolatile memory concerning the gestalt of operation of the 4th of this invention is explained using drawing 21 and drawing 22 . Drawing 21 is the cross section of the nonvolatile memory explaining write-in actuation. Drawing 22 is the cross section of the nonvolatile memory explaining elimination actuation. As shown in drawing 21 , at the time of the writing of a memory cell, about 5V is impressed to Gate G, and about -5V is impressed to Drain D, respectively, and let Source S be floating potential. Thus, voltage is impressed, energy is given to the electron of the tunneling reason between band-bands by the electric field near the drain field, and an electron is poured into charge accumulation layer 4b by the side of a drain field. the case where an electron is poured into charge accumulation layer 4a by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above On the other hand, as shown in drawing 22 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using FN current. Moreover, when Gate G is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, let Source S and Drain D be the n-type-semiconductor substrate 19, this potential, or floating potential.

[0051] The writing of a memory cell can be carried out even if it uses a channel thermoelectron like [in the case of the gestalt of operation of the 2nd of this invention]. In this case, about -2.5V is impressed to Gate G, about -5V is impressed to Drain D, respectively, and Source S is grounded. Thus, voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field with a channel thermoelectron. the case where an electron is poured into charge accumulation layer 4a by the side of a source field on the other hand -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress

[0052] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0053] (Gestalt of the 5th operation) Next, the gestalt of operation of the 5th of this invention is explained. Generally, a circumference circuit is arranged in semiconductor memory around a memory cell array. For example, there are a decoder, writing/elimination circuit, a readout circuitry, an analog circuit, various kinds of I/O circuits, various kinds of capacitor circuits, etc. as the circumference circuit. The gestalt of operation of the 5th of this invention shows the example which manufactures simultaneously the MOS transistor which constitutes these circumference circuit using the manufacturing process of the memory cell transistor of the gestalt of the 2nd - the 4th operation. Drawing 23 is the cross section showing the structure of the MOS transistor which constitutes the circumference circuit of the non-volatile semiconductor memory concerning the gestalt of operation of the 5th of this invention. As shown in drawing 23 , according to the gestalt of operation of the 5th of this invention, seven kinds of MOS transistors (Tr1-Tr7) from which a gate insulator layer differs in addition to a memory cell transistor (memory cell Tr) are realizable. In addition, the memory cell transistor of drawing 23 is a memory cell transistor shown in drawing 10 . Moreover, MOS transistors Tr1-Tr7 show n mold MOS transistor altogether. n-mold diffusion layer 10 of a memory cell transistor and n+ mold diffusion layer 11, and the conductive layer 12 are omitted in order to make a drawing legible. The same is said of MOS transistors Tr1-Tr7.

[0054] Next, the manufacture method of the MOS transistor shown in drawing 23 is explained using drawing 24 thru/or drawing 30 . it is first shown in drawing 24 -- as -- the p type semiconductor substrate 1 whole surface -- JVD -- the small silicon nitride of charge storage capacity is deposited by law, and the about 10nm 1st gate insulator layer 13 is formed. Well-known exposure technology and dry etching technology remove the 1st gate insulator layer 13 of some fields on the p type semiconductor substrate 1 after 1st gate insulator layer 13 formation. And as shown in drawing 25 , silicon oxide is deposited with a CVD method and the about 5-10nm 2nd gate insulator layer 14 is formed. Exposure technology and dry etching technology remove the 2nd gate insulator layer 14 of some fields after 2nd gate insulator layer 14 formation. then, it is shown in drawing 26 -- as -- JVD -- the small silicon nitride of charge storage capacity is deposited by law, and the about 10nm 3rd gate insulator layer 15 is formed. Exposure technology and dry etching

technology remove the 3rd gate insulator layer 15 of some fields after 3rd gate insulator layer 15 formation. Thus, seven kinds of gate insulator layers which consist of at least one of the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layers 15 are realized.

[0055] next, it is shown in drawing 27 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and two or more gate electrodes 3 are formed. Furthermore, the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms each source field and drain field of a memory cell transistor and an MOS transistor by dry etching by using the gate electrode 3 as a mask are removed.

[0056] Next, as shown in drawing 28 , wet etching of the field which forms a bonnet and a memory cell transistor for the field which forms MOS transistors Tr1-Tr7 by the photoresist 22 is carried out. An etching reagent uses what has the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. The edge of the 2nd gate insulator layer 14 of the field which forms a memory cell transistor by this wet etching is etched selectively, and the space 17 for charge accumulation layer formation is formed. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 5th of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. and it is shown in drawing 29 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- it deposits so that the space 17 for charge accumulation layer formation may be thoroughly embedded by law in the high silicon nitride 18 of charge storage capacity. Then, as shown in drawing 30 , anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of high silicon nitrides of charge storage capacity are formed in the field which forms a memory cell transistor. The subsequent process is the same as the gestalt of operation of the 2nd of this invention.

[0057] According to the gestalt of operation of the 5th of this invention, seven kinds of MOS transistors Tr1-Tr7 which have the gate insulator layer from which thickness differs can be manufactured to a memory cell transistor and coincidence. Thereby, the MOS transistor corresponding to operating voltage various from the high resisting pressure transistor of high-tension actuation to a super-low voltage actuation transistor can be offered. Furthermore, n mold MOS transistor and p mold MOS transistor are realizable. Moreover, the gate electrode 3 of a memory cell transistor and MOS transistors Tr1-Tr7 consists of same materials, and is formed at the same exposure process and a dry etching process. Therefore, a detailed transistor with few alignment gaps of a photo mask can be offered.

[0058] (Gestalt of the 6th operation) Next, the gestalt of operation of the 6th of this invention is explained. the gestalt of this 6th operation shows the example which writes in electrically, writes in and carries out reading appearance to eliminable nonvolatile memory and an eliminable high speed, and realizes possible volatile memory on the same chip. The cross section showing the memory cell structure of the nonvolatile memory carried in the semiconductor memory which drawing 31 requires for the gestalt of operation of the 6th of this invention, and drawing 32 are the cross sections showing the memory cell structure of the volatile memory carried in the semiconductor memory concerning the gestalt of operation of the 6th of this invention. The nonvolatile memory of drawing 31 and the volatile memory of drawing 32 are loaded together on the same chip.

[0059] (A) As shown in nonvolatile memory drawing 31 , the memory cell of the nonvolatile memory concerning the gestalt of this 6th operation consists of n mold MOS transistors. And with the memory cell structure of this nonvolatile memory, the 2nd gate insulator layer 14 is formed through the 1st gate insulator layer 13 on the principal plane of the p type semiconductor substrate 1. The charge accumulation layer 4 (4a, 4b) is formed in the ends of the 2nd gate insulator layer 14. On the 2nd gate insulator layer 14 and the charge accumulation layer 4, the gate electrode 3 is formed through the 3rd gate insulator layer 15. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.

[0060] The memory cell of the nonvolatile memory concerning the gestalt of operation of the 6th of this invention has the LDD structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And it consists of three-layer cascade screens which a gate insulator layer turns into from the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer), and the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layer 4 (4a, 4b) is formed in the both ends of the 2nd gate insulator layer 14. An electron is accumulated in these two charge accumulation layers 4a and 4b. That are recording condition (1) charge accumulation layer 4a, All of 4b can take the

condition which is not accumulating the electron, the condition that only (2) charge accumulation layer 4a is accumulating the electron, the condition that only (3) charge accumulation layer 4b is accumulating the electron, and four conditions of condition ** that (4) charge accumulation layers 4a and 4b are accumulating the electron. A changed part of the threshold voltage produced by the existence of the electron held in these two charge accumulation layers 4a and 4b is made to correspond to "00" of storage information, "01", "10", and "11." Moreover, with this memory cell structure, since the charge accumulation layer 4 is located above the channel field edge, the threshold voltage of a channel field center section is decided only by high impurity concentration of a channel field, and it does not depend for it on the are recording condition of the electron of the charge accumulation layer 4. Therefore, fault elimination (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and cannot produce the poor leak which originates in fault elimination by that cause, a poor program, and poor read-out. Moreover, the leakage current between a source field and a drain field can be controlled only with gate voltage, and can realize highly reliable nonvolatile memory. What is necessary is for the charge accumulation layer 4 just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm, induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0061] Although n-mold diffusion layer 10 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the nonvolatile memory concerning the gestalt of operation of the 6th of this invention, a source field and a drain field may consist of single drain structure and double drain structure. Although the 2nd gate insulator layer 14 prevents leak between charge accumulation layer 4a-4b, it can consist of silicon oxide, for example. Moreover, if the metal oxide film which has a high dielectric constant is used for the 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved. As a metal oxide film, there are TiO2, Ta 2O5, aluminum2O5, and PZT and SBT.

[0062] Next, actuation of the non-volatile semiconductor memory concerning the gestalt of operation of the 6th of this invention is explained using drawing 33 and drawing 34 . Drawing 33 is the cross section of the nonvolatile memory explaining write-in actuation. Drawing 34 is the cross section of the nonvolatile memory explaining elimination actuation. As shown in drawing 33 , at the time of the writing of a memory cell, about 7-8V is impressed to Gate G, about 5V is impressed to Drain D, respectively, and Source S is grounded. Thus, voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field with a channel thermoelectron (CHE). the case where an electron is poured into charge accumulation layer 4b by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above On the other hand, as shown in drawing 34 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using Fowler Nordheim (FN) mold tunnel current. Moreover, when Gate G is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, what is necessary is just to let Source S and Drain D be the p type semiconductor substrate 1 and this potential. Moreover, it is also possible to impress different positive voltage from the potential of the p type semiconductor substrate 1 to a drain electrode, and to draw out an electron for a source electrode only from charge accumulation layer 4b by the side of floating potential (Floating), then a drain electrode. What is necessary is to impress positive voltage to a source electrode, in drawing out an electron only from charge accumulation layer 4a by the side of a source electrode, and just to let a drain electrode be floating potential.

[0063] The writing of a memory cell can also be performed like elimination of a memory cell using FN current. About 10V is impressed between Gate G and the p type semiconductor substrate 1, and an electron is poured into the charge accumulation layers 4a and 4b with FN current. In this case, an electron can be simultaneously injected into two or more memory cells in which Gate G is common.

[0064] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just

choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0065] (B) As shown in volatile memory drawing 32 , the memory cell of the volatile memory concerning the gestalt of operation of the 6th of this invention consists of n mold MOS transistors. With the memory cell structure of this volatile memory, the 2nd gate insulator layer 14 of drawing 31 is directly arranged on the principal plane of the p type semiconductor substrate 1. And although the charge accumulation layer 4 (4c, 4d) is formed in the ends of the 2nd gate insulator layer 14 like the nonvolatile memory of drawing 31 , it differs from the nonvolatile memory of drawing 31 in that these charge accumulation layers 4c and 4d are arranged on the principal plane of the p type semiconductor substrate 1 through the tunnel insulator layer 23. On the 2nd gate insulator layer 14 and the charge accumulation layer 4, the gate electrode 3 is formed through the 3rd gate insulator layer 15. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.

[0066] The memory cell of the volatile memory concerning the gestalt of operation of the 6th of this invention has the LDD structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And a gate insulator layer consists of the 2nd gate insulator layer 14, a tunnel insulator layer 23, and the 3rd gate insulator layer 15, and the charge accumulation layer 4 is formed in the both ends of the 2nd gate insulator layer 14. An electron is accumulated in these two charge accumulation layers 4c and 4d. That are recording condition (1) charge accumulation layer 4c, 4d all can take four conditions of the condition which is not accumulating the electron, the condition that only (2) charge accumulation layer 4c is accumulating the electron, the condition that only 4d of (3) charge accumulation layers is accumulating the electron, (4) charge accumulation layer 4c, and condition ** that is accumulating both 4d of electrons. A changed part of the threshold voltage produced by the existence of the electron held in these two charge accumulation layers 4c and 4d is made to correspond to "00" of storage information, "01", "10", and "11." Moreover, with this memory cell structure, since the charge accumulation layer 4 is located above the channel field edge, the threshold voltage of a channel field center section is decided only by high impurity concentration of a channel field, and it does not depend for it on the are recording condition of the electron of the charge accumulation layer 4. Therefore, fault elimination (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and cannot produce the poor leak which originates in fault elimination by that cause, a poor program, and poor read-out. Moreover, the leakage current between a source field and a drain field can be controlled only with gate voltage, and can realize highly reliable volatile memory. What is necessary is for the charge accumulation layer 4 just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 3rd gate insulator layer 15 is constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm, induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0067] Although n-mold diffusion layer 10 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the volatile memory concerning the gestalt of operation of the 6th of this invention, a source field and a drain field may consist of single drain structure and double drain structure. Although the 2nd gate insulator layer 14 prevents the leak for charge accumulation layer 4c-4d, it can consist of silicon oxide, for example. Moreover, if the metal oxide film which has a high dielectric constant is used for the 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved. As a metal oxide film, there are TiO2, Ta 2O5, aluminum2O5, and PZT and SBT.

[0068] In the volatile memory concerning the gestalt of operation of the 6th of this invention, the tunnel insulator layer 23 is arranged in the charge accumulation layers [4c and 4d] lower part. The tunnel insulator layer 23 consists of silicon oxide of a thin film which has the thickness in which direct tunneling is possible, and makes possible read-out

write-in [high-speed] in 100 or less ns required of a dynamic RAM. When the tunnel insulator layer 23 is constituted from silicon oxide, the thickness is just 3nm or less. Moreover, if constituted from a silicon nitride 3nm or less, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is about 1.5nm. Since the electrons accumulated in the charge accumulation layer 4 by the leakage current through the tunnel insulator layer 23 decrease in number gradually, prolonged data-hold is difficult in practice. However, re-writing is possible enough within the refresh period of the usual dynamic RAM, and I think that it is satisfactory at all in actuation as a dynamic RAM. This is shown to 1995IEDM digest p.867 by C.H-J.Wann and others.

[0069] Reading of a memory cell is performed by detecting the read-out current which flows between a source electrode and drain electrodes. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to a charge accumulation layers [4c and 4d] are recording condition. To which bias shall be carried out between a source electrode and a drain electrode should just choose the direction where the modulation of current transfer characteristics appears notably. According to four charge accumulation layers [4c and 4d] are recording conditions, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0070] Furthermore, if the volatile memory concerning the gestalt of operation of the 6th of this invention does not pour a charge into the charge accumulation layers 4c and 4d, it is possible to make it operate as a usual MOS transistor.

[0071] (C) Explain the manufacture method of the memory cell of the nonvolatile memory concerning the manufacture method of a non-volatile and volatile mixed-loading memory, next the gestalt of operation of the 6th of this invention, and volatile memory using drawing 35 thru/or drawing 43 and drawing 44 thru/or drawing 52 . The cross section, drawing 44 , or drawing 52 which shows the manufacture method of the nonvolatile memory which drawing 35 thru/or drawing 43 require for the gestalt of operation of the 6th of this invention is the cross section showing the manufacture method of the volatile memory concerning the gestalt of operation of the 6th of this invention.

[0072] As first shown in drawing 35 and drawing 44 , the small silicon nitride of charge storage capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. The nonvolatile memory formation field of drawing 35 is removed by the photoresist after 1st gate insulator layer 13 formation by the wet etching [insulator layer / 13 / of a bonnet and the volatile memory formation field of drawing 44 / 1st gate] method for example, using a heating phosphoric acid solution. Therefore, the 1st gate insulator layer 13 is formed only in the nonvolatile memory formation field of drawing 35 . Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method.

[0073] Next, as shown in drawing 36 and drawing 45 , silicon oxide is deposited all over p type semiconductor substrate 1 with a CVD method, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed. After all, the 1st, 2nd, and 3rd gate insulator layers 13, 14, and 15 are formed in the nonvolatile memory formation field of drawing 36 , and the 2nd and 3rd gate insulator layers 14 and 15 are formed in the volatile memory formation field of drawing 45 .

[0074] next, it is shown in drawing 37 and drawing 46 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, in the nonvolatile memory formation field of drawing 37 , dry etching of the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms a source field and a drain field is carried out in self align by using the gate electrode 3 as a mask. On the other hand, in the volatile memory formation field of drawing 46 , dry etching of the 2nd gate insulator layer 14 and the 3rd gate insulator layer 15 is carried out in self align.

[0075] Next, as shown in drawing 38 and drawing 47 , the space 17 for charge accumulation layer formation is formed. This space 17 is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. The space 17 for charge accumulation layer formation of the space 17 for charge accumulation layer formation of the nonvolatile memory formation field of drawing 38 and the volatile memory formation field of drawing 47 is formed simultaneously. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 6th of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. Moreover, this space 17 may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.

[0076] Next, as shown in drawing 39 and drawing 48 , it oxidizes by the RTO method and the tunnel insulator layer 23

which consists of the silicon oxide which can be tunneled direct is formed for the p type semiconductor substrate 1 whole surface.
[0077] next, it is shown in drawing 40 and drawing 49 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- it deposits so that the space 17 for charge accumulation layer formation may be thoroughly embedded by law in the high silicon nitride 18 of charge storage capacity. And as shown in drawing 41 and drawing 50 , anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layer 4 (4a, 4b, 4c, 4d) which consisted of high silicon nitrides of charge storage capacity is formed simultaneously.
[0078] Next, as shown in drawing 42 and drawing 51 , after forming an oxide film 16 all over p type semiconductor substrate 1, n-mold diffusion layer 10 of low high impurity concentration is formed. It forms by activating the impurity which n-mold diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0079] Next, as shown in drawing 43 and drawing 52 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, n+ mold diffusion layer 11 of high high impurity concentration is formed. It forms by activating the impurity which n+ mold diffusion layer 11 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0080] and the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere -- the gate electrode 3 and n+ mold diffusion layer 11 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure of the volatile memory shown in the nonvolatile memory shown in drawing 31 and drawing 32 will be completed.
[0081] In addition, although a graphic display is not carried out, the semiconductor device which carried final nonvolatile memory and volatile memory is completed after memory cell structure completion of drawing 31 and drawing 32 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.
[0082] Thus, with the gestalt of the 6th operation of this invention, the charge accumulation layer 4 (4a, 4b, 4c, 4d) can be formed in the lower part of the ends of the gate electrode 3 in self align. Therefore, detailed-ization of the direction of gate length of drawing 31 and the memory cell transistor of drawing 32 is attained. Thereby, the nonvolatile memory and volatile memory of large capacity and high density can be offered. Moreover, the cel area per bit is mostly reduced by half compared with the former, and the nonvolatile memory and volatile memory which were reduced substantially can be realized.
[0083] The width of face of the direction of channel length of the charge accumulation layer 4 is easily controllable by accommodation of the etching speed difference of the p type semiconductor substrate 1, the 1st gate insulator layer 13 and the 3rd gate insulator layer 15, and the 2nd gate insulator layer 14, and etching time. Thereby, the charge accumulation layer 4 can be arranged to the symmetry. And since the 2nd gate insulator layer 14 dissociates thoroughly electrically between the charge accumulation layers 4, the interaction between the charge accumulation layers 4 does not happen. Furthermore, from a source field, a drain field, the gate electrode 3, and a channel field, since it is thoroughly insulated with the 1st insulator layer 13, tunnel insulator layer 23, 3rd insulator layer 15, and oxide film 16, the charge accumulation layer 4 can offer the nonvolatile memory and volatile memory which were excellent in the charge maintenance property. It is extended and formed in the direction of a channel field from the edge of the gate electrode 3, and the charge accumulation layer 4 is current transfer-characteristics ********** of a memory cell by the charge storage condition of the portion by the side of the channel field of the charge accumulation layers 4. Therefore, if the gate length lay length of this portion is reduced to a limit, more detailed nonvolatile memory and volatile memory can be offered.
[0084] Since the cellular structure is easily realizable at the usual CMOS process, nonvolatile memory and volatile memory can be manufactured by low cost using the existing production line.
[0085] Furthermore, since the greater part of the manufacturing process is communalized, it is low cost, and above-mentioned nonvolatile memory and volatile memory are a short manufacture construction period, and can manufacture the semiconductor device consolidated with nonvolatile memory and volatile memory.
[0086] In addition, with the gestalt of operation of the 6th of this invention, although a silicon nitride and the 2nd gate insulator layer 14 are constituted from silicon oxide and the 3rd gate insulator layer 15 is constituted for the 1st gate insulator layer 13 from a silicon nitride, silicon oxide and the 2nd gate insulator layer 14 may be consisted of from a silicon nitride, and the 3rd gate insulator layer 15 may consist of silicon oxide for the 1st gate insulator layer 13. In this case, the 1st gate insulator layer 13 consists of about 10nm silicon oxide which oxidized thermally the p type

semiconductor substrate 1. the 2nd gate insulator layer 14 -- JVD -- it constitutes from a low silicon nitride of the about 5-10nm charge storage capacity deposited by law. What is necessary is for the 3rd gate insulator layer 15 just to consist of about 10nm silicon oxide deposited with the CVD method. Moreover, since formation of the space 17 for charge accumulation layer formation constitutes the 1st gate oxide 13 and the 3rd gate insulator layer 15 from silicon oxide and constitutes the 2nd gate insulator layer 14 from a silicon nitride, it should just use for example, a phosphoric-acid system as an etching reagent.

[0087] (Gestalt of the 7th operation) Next, the gestalt of operation of the 7th of this invention is explained. the gestalt of this 7th operation shows the example which writes in electrically, writes in and carries out reading appearance to eliminable nonvolatile memory and an eliminable high speed like the gestalt of the 6th operation of the above, and realizes possible volatile memory on the same chip. The cross section showing the memory cell structure of the nonvolatile memory carried in the semiconductor memory which drawing 53 requires for the gestalt of operation of the 7th of this invention, and drawing 54 are the cross sections showing the memory cell structure of the volatile memory carried in the semiconductor memory concerning the gestalt of operation of the 7th of this invention. The nonvolatile memory of drawing 53 and the volatile memory of drawing 54 are loaded together on the same chip. Since it is the same as that of the gestalt of the 6th operation of the above about the nonvolatile memory shown in drawing 53 , the explanation is omitted here.

[0088] As shown in drawing 54 , the memory cell of the volatile memory concerning the gestalt of this 7th operation consists of n mold MOS transistors. And with the memory cell structure of this volatile memory, charge accumulation layer 4e is arranged through the tunnel insulator layer 23 on the principal plane of the p type semiconductor substrate 1. On charge accumulation layer 4e, the gate electrode 3 is formed through the 4th gate insulator layer 24. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.

[0089] The memory cell of the volatile memory concerning the gestalt of operation of the 7th of this invention has the LDD structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And it consists of laminated structures to which a gate insulator layer changes from the tunnel insulator layer 23 and the 4th gate insulator layer 21, and charge accumulation layer 4e is arranged between the tunnel insulator layer 23 and the 4th gate insulator layer 24. An electron is accumulated in this charge accumulation layer 4e, and a changed part of the threshold voltage produced by the existence of the electron held at this charge accumulation layer 4e is made to correspond to "0" of storage information, and "1." What is necessary is for charge accumulation layer 4e just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 4th gate insulator layer 24 is constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm, induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0090] Although n-mold diffusion layer 10 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the volatile memory concerning the gestalt of operation of the 7th of this invention, a source field and a drain field may consist of single drain structure and double drain structure.

[0091] In the volatile memory concerning the gestalt of operation of the 7th of this invention, the tunnel insulator layer 23 is arranged in the lower part of charge accumulation layer 4e. The tunnel insulator layer 23 consists of silicon oxide of a thin film which has the thickness in which direct tunneling is possible, and read-out write-in [high-speed] of it in 100 or less ns required of a dynamic RAM becomes possible. When the tunnel insulator layer 23 is constituted from silicon oxide, the thickness is just 3nm or less. Moreover, if constituted from a silicon nitride 3nm or less, silicon oxide conversion thickness can stabilize for it and realize the very thin tunnel insulator layer 23 which is about 1.5nm.

[0092] Furthermore, if the volatile memory concerning the gestalt of operation of the 7th of this invention does not pour

a charge into charge accumulation layer 4e, it is possible to also make it operate as a usual MOS transistor.
[0093] Next, the manufacture method of the memory cell of the nonvolatile memory concerning the gestalt of operation of the 7th of this invention and volatile memory is explained using drawing 55 thru/or drawing 62 and drawing 63 thru/or drawing 70 . The cross section, drawing 63 , or drawing 70 which shows the manufacture method of the nonvolatile memory which drawing 55 thru/or drawing 62 require for the gestalt of operation of the 7th of this invention is the cross section showing the manufacture method of the volatile memory concerning the gestalt of operation of the 7th of this invention.
[0094] As first shown in drawing 55 and drawing 63 , the small silicon nitride of charge storage capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method. Silicon oxide is deposited with a CVD method after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
[0095] next, it is shown in drawing 56 and drawing 64 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, in the nonvolatile memory formation field of drawing 56 , patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, dry etching of the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask is carried out in self align. In the volatile memory formation field of drawing 64 , a polycrystalline silicon film, the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layer 15 are removed altogether, and p type semiconductor substrate 1 front face exposes them.
[0096] Next, as shown in drawing 57 , in a nonvolatile memory formation field, the space 17 for charge accumulation layer formation is formed. The space 17 for this charge accumulation layer formation is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 7th of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. Moreover, the space 17 for charge accumulation layer series formation may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas. On the other hand, as shown in drawing 65 , in the volatile memory formation field, the front face of the p type semiconductor substrate 1 has been exposed.
[0097] next, it is shown in drawing 58 and drawing 66 -- as -- the p type semiconductor substrate 1 whole surface -- for example, RTO -- the tunnel insulator layer 23 which is alike with law and consists of the silicon oxide which can be tunneled direct is formed. after tunnel insulator layer 23 formation and the p type semiconductor substrate 1 whole surface -- LPCVD -- the high silicon nitride 18 of charge storage capacity is deposited by law. At this time, the space 17 for charge accumulation layer formation is thoroughly embedded by the silicon nitride 18. And as shown in drawing 59 , in a nonvolatile memory formation field, anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layer 4 (4a, 4b) which consisted of high silicon nitrides 18 of charge storage capacity is formed. In that case, the volatile memory formation field of drawing 67 is covered by the photoresist, and the silicon nitride 18 is not etched.
[0098] Silicon oxide is deposited all over p type semiconductor substrate 1 after etching termination of the silicon nitride 18, and the 4th gate insulator layer 24 is formed. Here, the 4th gate insulator layer 24 of the nonvolatile memory formation field of drawing 59 is removed. The clearance is performed by etching the 4th gate insulator layer 24 which deposited the volatile memory formation field of drawing 67 on the bonnet and the nonvolatile memory formation field of drawing 59 in the photoresist.
[0099] next, it is shown in drawing 68 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law is deposited. And patterning of the polycrystalline silicon film is carried out with exposure technology and etching technology, and gate electrode 3a is formed. Then, dry etching of the tunnel insulator layer 23 of the front face of the p type semiconductor substrate 1 of the field which forms a source field and a drain field, charge accumulation layer 4e, and the 4th gate insulator layer 24 is carried out in self align by using gate electrode 3a as an etching mask. On the other hand, in a nonvolatile memory formation field, as shown in drawing 60 , all polycrystalline silicon films may be removed, patterning may be carried out according to the gate electrode 3, and a new gate electrode may be formed.

[0100] Next, as shown in drawing 61 and drawing 69 , after forming an oxide film 16 all over p type semiconductor substrate 1, n-mold diffusion layer 10 of low high impurity concentration is formed. It forms by activating the impurity which n-mold diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0101] Next, as shown in drawing 62 and drawing 70 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, n+ mold diffusion layer 11 of high high impurity concentration is formed. It forms by activating the impurity which n+ mold diffusion layer 11 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0102] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere -- the gate electrode 3 and n+ mold diffusion layer 11 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure of the volatile memory shown in the nonvolatile memory shown in drawing 53 and drawing 54 will be completed.
[0103] Although a graphic display is not carried out, a final non-volatile memory cell and an volatile memory cell are completed after memory cell structure completion of drawing 53 and drawing 54 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.
[0104] With the gestalt of operation of the 7th of this invention, although a silicon nitride and the 2nd gate insulator layer 14 are constituted from silicon oxide and the 3rd gate insulator layer 15 is constituted for the 1st gate insulator layer 13 from a silicon nitride, silicon oxide and the 2nd gate insulator layer 14 may be consisted of from a silicon nitride, and the 3rd gate insulator layer 15 may consist of silicon oxide for the 1st gate insulator layer 13. In this case, the 1st gate insulator layer 13 consists of about 10nm silicon oxide which oxidized thermally the p type semiconductor substrate 1. the 2nd gate insulator layer 14 -- JVD -- it constitutes from a low silicon nitride of the about 5-10nm charge storage capacity deposited by law. What is necessary is for the 3rd gate insulator layer 15 just to consist of about 10nm silicon oxide deposited with the CVD method. Moreover, since formation of the space 17 for charge accumulation layer formation constitutes the 1st gate oxide 13 and the 3rd gate insulator layer 15 from silicon oxide and constitutes the 2nd gate insulator layer 14 from a silicon nitride, it should just use for example, a phosphoric-acid system as an etching reagent.
[0105] Although both the memory cells of nonvolatile memory and volatile memory explained the example which consists of n mold MOS transistors with the gestalt of the 6th and operation of the 7th of this invention, of course, you may be the memory cell of p mold MOS transistor of a reverse conductivity type. In this case, what is necessary is just to read the electric conduction type of a substrate or a diffusion layer as a reverse thing suitably in the above-mentioned explanation.
[0106] (Gestalt of the 8th operation) Next, the gestalt of operation of the 8th of this invention is explained. With the gestalt of the above-mentioned 1st thru/or the 7th operation, the structure of a charge accumulation layer does not contribute to improvement in electronic injection efficiency directly. In the non-volatile semiconductor memory of floating-gate structure, a level difference is prepared in a channel portion and the attempt which raises electronic injection efficiency is proposed (S. Ogura, 1998IEDM, p987, United States Patent number No. 5780341). However, in order to adopt floating-gate structure by this proposal, to the defect and leak site in an oxide film, it is weak. Moreover, there is a possibility that sufficient reliability cannot be acquired, also to the defect which may be generated at the time of level difference structure formation. The gestalt of operation of the 8th of this invention is an easy process, and can raise electronic injection efficiency.
[0107] Drawing 71 is the cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 8th of this invention. The gestalt of this 8th operation is establishing a level difference and dip in the channel field of a memory cell, and aims at improvement in the electronic injection efficiency at the time of writing. As shown in drawing 71 , this memory cell consists of n mold MOS transistors. And with the structure of the memory cell concerning the gestalt of this 8th operation, the 2nd gate insulator layer 14 is formed in the front face of the p type semiconductor substrate 1 through the 1st gate insulator layer 13. The charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14. On the 2nd gate insulator layer 14 and charge accumulation layer 4a, and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the p type semiconductor substrate 1

of the lower part of this sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.

[0108] Furthermore, with the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 8th of this invention, a level difference 26 is formed in the channel field 25. With this level difference 26, the charge accumulation layer 4 will be located in the dispersion direction of the electron in the p type semiconductor substrate 1. Therefore, the injection efficiency of the electron at the time of writing improves.

[0109] The memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 8th of this invention has the LDD structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And it consists of three-layer cascade screens which a gate insulator layer turns into from the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer), and the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14. An electron is accumulated in these two charge accumulation layers 4a and 4b. That are recording condition (1) charge accumulation layer 4a, All of 4b can take the condition which is not accumulating the electron, the condition that only (2) charge accumulation layer 4a is accumulating the electron, the condition that only (3) charge accumulation layer 4b is accumulating the electron, and four conditions of condition ** that (4) charge accumulation layers 4a and 4b are accumulating the electron. A changed part of the threshold voltage produced by the existence of the electron held in these two charge accumulation layers 4a and 4b is made to correspond to "00" of storage information, "01", "10", and "11." Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located above the channel field edge, the threshold voltage of a channel field center section is decided only by high impurity concentration of a channel field, and they do not depend for it on the are recording condition of the electron of the charge accumulation layers 4a and 4b. Therefore, fault elimination (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and cannot produce the poor leak which originates in fault elimination by that cause, a poor program, and poor read-out. Moreover, the leakage current between a source field and a drain field can be controlled only with gate voltage, and can realize highly reliable non-volatile semiconductor memory. What is necessary is for the charge accumulation layers 4a and 4b just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm, induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0110] Although n-mold diffusion layer 10 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 8th of this invention, a source field and a drain field may consist of single drain structure and double drain structure. Although the 2nd gate insulator layer 14 prevents leak between charge accumulation layer 4a-4b, it can consist of silicon oxide, for example. Moreover, if the metal oxide film which has a high dielectric constant is used for the 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved. As a metal oxide film, there are TiO2, Ta 2O5, aluminum2O5, and PZT and SBT.

[0111] With the gestalt of operation of the 8th of this invention, although the level difference 26 was formed in both by the side of the source and a drain, you may prepare only in either. Especially the memory that memorizes the information for 1 bit is enough if there is only one side.

[0112] Next, actuation of the nonvolatile memory concerning the gestalt of operation of the 8th of this invention is explained using drawing 72 and drawing 73 . Drawing 72 is the cross section of the nonvolatile memory explaining write-in actuation. Drawing 73 is the cross section of the nonvolatile memory explaining elimination actuation. As shown in drawing 72 , at the time of the writing of a memory cell, about 6-8V is impressed to Gate G, about 4-5V is impressed to Drain D, respectively, and Source S is grounded. Thus, voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field with a channel thermoelectron (CHE). By having formed the level difference 26 in the channel field 25, it is located in the electronic dispersion direction at charge accumulation layer 4b. For this reason, the injection efficiency of the electron to charge accumulation layer 4b can improve, and

improvement in the speed of grouting velocity and reduction-ization of applied voltage can be attained. the case where an electron is poured into charge accumulation layer 4a by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above-mentioned case On the other hand, as shown in drawing 73 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using Fowler Nordheim (FN) mold tunnel current. Moreover, when the gate electrode 3 is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, what is necessary is just to let Source S and Drain D be the p type semiconductor substrate 1 and this potential. Moreover, it is also possible to impress different positive voltage from the potential of the p type semiconductor substrate 1 to Drain D, and to draw out an electron for Source S only from charge accumulation layer 4a by the side of floating potential (Floating), then Drain D. What is necessary is to impress positive voltage to Source S, in drawing out an electron only from charge accumulation layer 4b by the side of Source S, and just to let Drain D be floating potential.

[0113] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0114] Next, the manufacture method of the memory cell of the nonvolatile memory concerning the gestalt of operation of the 8th of this invention is explained using drawing 74 thru/or drawing 82 . As first shown in drawing 74 , the wrap photoresist pattern 27 is formed for the field in which the channel field 25 is formed on the p type semiconductor substrate 1. And as shown in drawing 75 , a level difference 26 is formed by etching the p type semiconductor substrate 1 by the RIE method.

[0115] Next, as shown in drawing 76 , the small silicon nitride of charge storage capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method. Silicon oxide is deposited with a CVD method after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.

[0116] next, it is shown in drawing 77 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, dry etching of the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask is carried out in self align.

[0117] Next, as shown in drawing 78 , the space 17 for charge accumulation layer formation is formed. This space 17 is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 8th of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. Moreover, the space 17 for charge accumulation layer formation may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.

[0118] next, it is shown in drawing 79 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- it deposits so that the space 17 for charge accumulation layer formation may be thoroughly embedded by law in the high silicon nitride 18 of charge storage capacity. And as shown in drawing 80 , anisotropic etching by RIE is performed to the p type semiconductor substrate 1 whole surface, and the charge accumulation layers 4a and 4b which consisted of high silicon nitrides of charge storage capacity are formed.

[0119] Next, as shown in drawing 81 , after forming an oxide film 16 all over p type semiconductor substrate 1, n-mold diffusion layer 10 of low high impurity concentration is formed. It forms by activating the impurity which n-mold diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.

[0120] Next, as shown in drawing 82 , after forming the sidewall spacer 9 in the side attachment wall of the gate

electrode 3, n+ mold diffusion layer 11 of high high impurity concentration is formed. It forms by activating the impurity which n+ mold diffusion layer 11 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0121] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere -- the gate electrode 3 and n+ mold diffusion layer 11 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 71 will be completed.
[0122] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 71 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.
[0123] Thus, with the gestalt of the 8th operation of this invention, the charge accumulation layers 4a and 4b can be formed in the lower part of the ends of the gate electrode 3 in self align. Therefore, detailed-ization of the direction of gate length of a cel transistor is attained. Thereby, large capacity and the non-volatile semiconductor memory of high density can be offered. Moreover, the cel area per bit is mostly reduced by half compared with the former, and non-volatile semiconductor memory reduced substantially can be realized.
[0124] Moreover, the width of face of the direction of channel length of the charge accumulation layers 4a and 4b is easily controllable by accommodation of the etching speed difference of the 1st gate insulator layer 13 and the 3rd gate insulator layer 15, and the 2nd gate insulator layer 14, and etching time. Thereby, the charge accumulation layers 4a and 4b can be arranged to the symmetry. And since the charge accumulation layers 4a and 4b are electrically separated thoroughly by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b does not happen. Furthermore, since the charge accumulation layers 4a and 4b are thoroughly insulated from a source field, a drain field, the gate electrode 3, and a channel field with the 1st insulator layer 13 and the 3rd insulator layer 15, and an oxide film 16, the non-volatile semiconductor memory which was excellent in the charge maintenance property can be offered. It is extended and formed in the direction of a channel field from the edge of the gate electrode 3, and the charge accumulation layers 4a and 4b are current transfer-characteristics ********** of a memory cell by the charge storage condition of the portion by the side of the channel field of the charge accumulation layers 4a and 4b. Therefore, if the gate length lay length of this portion is reduced to a limit, more detailed non-volatile semiconductor memory can be offered.
[0125] Furthermore, since the cellular structure is easily realizable at the usual CMOS process, non-volatile semiconductor memory can be manufactured by low cost using the existing production line.
[0126] And with the gestalt of operation of the 8th of this invention, the electronic injection efficiency at the time of writing can be raised. For this reason, improvement in the speed of drawing speed and reduction-ization of the applied voltage at the time of writing can be attained.
[0127] (Gestalt of the 9th operation) Next, the gestalt of operation of the 9th of this invention is explained. In the gestalt of the 8th operation of the above, the gestalt of operation of the 9th of this invention made unnecessary the 2nd insulator layer 14 arranged between charge accumulation layer 4a of drawing 71 , and charge accumulation layer 4b, and has taken the configuration which made two charge accumulation layers 4a and 4b unify. Drawing 83 is the cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 9th of this invention. As shown in drawing 83 , this memory cell structure is changed to the charge accumulation layers 4a and 4b of the gestalt of the 8th operation of the above, and the 2nd insulator layer 14, and arranges 4f of charge accumulation layers.
[0128] Next, the manufacture method of the memory cell of the nonvolatile memory concerning the gestalt of operation of the 9th of this invention is explained using drawing 84 thru/or drawing 89 . Like the gestalt of the 8th operation of the above, as first shown in drawing 84 , the wrap photoresist pattern 27 is formed for the field in which the channel field 25 is formed on the p type semiconductor substrate 1. And as shown in drawing 85 , a level difference 26 is formed by etching the p type semiconductor substrate 1 by the RIE method.
[0129] Next, as shown in drawing 86 , the small silicon nitride of charge storage capacity is deposited all over p type semiconductor substrate 1, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method. after 1st gate insulator layer 13 formation and LPCVD -- about 5-10nm of high silicon nitrides 18 of charge storage capacity is formed by law. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate

insulator layer 15 is formed.
[0130] next, it is shown in drawing 87 -- as -- the p type semiconductor substrate 1 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, dry etching of the 1st gate insulator layer 13, the surface silicon nitride 18, and the surface 3rd gate insulator layer 15 of the p type semiconductor substrate 1 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask is carried out in self align. Here, 4f of charge accumulation layers is formed.
[0131] Next, as shown in drawing 88 , after forming an oxide film 16 all over p type semiconductor substrate 1, n-mold diffusion layer 10 of low high impurity concentration is formed. It forms by activating the impurity which n-mold diffusion layer 10 used the gate electrode 3 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0132] Next, as shown in drawing 89 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, n+ mold diffusion layer 11 of high high impurity concentration is formed. It forms by activating the impurity which n+ mold diffusion layer 11 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in n mold impurity, and was poured in by subsequent heat treatment.
[0133] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the p type semiconductor substrate 1, then the p type semiconductor substrate 1 is heat-treated in an inert atmosphere -- the gate electrode 3 and n+ mold diffusion layer 11 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 83 will be completed.
[0134] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 83 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.
[0135] (Gestalt of the 10th operation) Next, the gestalt of operation of the 10th of this invention is explained. Drawing 90 is the cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 10th of this invention. Although the level difference was prepared in the ends of a channel field by making a channel field into a convex condition to a semiconductor substrate with the gestalt of the above-mentioned 8th and the 9th operation, a level difference is prepared in a channel field by making a channel field into a concave condition to a semiconductor substrate with the gestalt of this 10th operation. And the gestalt of this 10th operation also aims at improvement in the electronic injection efficiency at the time of writing by establishing a level difference and dip in the channel field of a memory cell.
[0136] As shown in drawing 90 , this memory cell consists of p mold MOS transistors. And with the structure of the memory cell concerning the gestalt of this 10th operation, the 2nd gate insulator layer 14 is formed in the front face of the n-type-semiconductor substrate 19 through the 1st gate insulator layer 13. The charge accumulation layers 4a and 4b are formed in the ends of the 2nd gate insulator layer 14. On the 2nd gate insulator layer 14 and charge accumulation layer 4a, and 4b, the gate electrode 3 is formed through the 3rd gate insulator layer 15. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and p-mold diffusion layer 20 of the low high impurity concentration which touches a channel field, and p+ mold diffusion layer 21 of the high high impurity concentration located in the outside of this p-mold diffusion layer 20 are formed in the n-type-semiconductor substrate 19 of the lower part of this sidewall spacer 9. the gate electrode 3 and p+ mold diffusion layer 21 -- a conductive layer 12 is formed in each front face.
[0137] Furthermore, with the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 10th of this invention, a level difference 26 is formed in the channel field 25. With this level difference 26, the charge accumulation layer 4 will be located in the dispersion direction of the electron in the p type semiconductor substrate 1. Therefore, the injection efficiency of the electron at the time of writing improves.
[0138] The memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 10th of this invention has the LDD structure which constituted the source field and the drain field from a p-mold diffusion layer 20 of low high impurity concentration, and a p+ mold diffusion layer 21 of high high impurity concentration. And it consists of three-layer cascade screens which a gate insulator layer turns into from the 1st gate insulator layer 13 (lower layer), the 2nd gate insulator layer 14 (interlayer), and the 3rd gate insulator layer 15 (upper layer), and the charge accumulation layers 4a and 4b are formed in the both ends of the 2nd gate insulator layer 14. An electron is accumulated in these two charge accumulation layers 4a and 4b. That are recording condition (1) charge accumulation layer 4a, All

of 4b can take the condition which is not accumulating the electron, the condition that only (2) charge accumulation layer 4a is accumulating the electron, the condition that only (3) charge accumulation layer 4b is accumulating the electron, and four conditions of condition ** that (4) charge accumulation layers 4a and 4b are accumulating the electron. A changed part of the threshold voltage produced by the existence of the electron held in these two charge accumulation layers 4a and 4b is made to correspond to "00" of storage information, "01", "10", and "11." Moreover, with this memory cell structure, since the charge accumulation layers 4a and 4b are located above the channel field edge, the threshold voltage of a channel field center section is decided only by high impurity concentration of a channel field, and they do not depend for it on the are recording condition of the electron of the charge accumulation layers 4a and 4b. Therefore, fault elimination (over-erase) by the excess and deficiency of the electron of the charge accumulation layers 4a and 4b is prevented, and cannot produce the poor leak which originates in fault elimination by that cause, a poor program, and poor read-out. Moreover, the leakage current between a source field and a drain field can be controlled only with gate voltage, and can realize highly reliable non-volatile semiconductor memory. What is necessary is for the charge accumulation layers 4a and 4b just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 1st gate insulator layer 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm, induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0139] Although p-mold diffusion layer 20 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 10th of this invention, a source field and a drain field may consist of single drain structure and double drain structure. Although the 2nd gate insulator layer 14 prevents leak between charge accumulation layer 4a-4b, it can consist of silicon oxide, for example. Moreover, if the metal oxide film which has a high dielectric constant is used for the 2nd gate insulator layer 14, the current transfer characteristics of the center of a channel field can be improved. As a metal oxide film, there are TiO2, Ta 2O5, aluminum2O5, and PZT and SBT.

[0140] With the gestalt of operation of the 10th of this invention, although the level difference 26 was formed in both by the side of the source and a drain, you may prepare only in either. Especially the memory that memorizes the information for 1 bit is enough if there is only one side.

[0141] Next, actuation of the nonvolatile memory concerning the gestalt of operation of the 10th of this invention is explained using drawing 91 and drawing 92 . Drawing 91 is the cross section of the nonvolatile memory explaining write-in actuation. Drawing 92 is the cross section of the nonvolatile memory explaining elimination actuation. As shown in drawing 91 , at the time of the writing of a memory cell, about 5V is impressed to Gate G, and about -5V is impressed to Drain D, respectively, and let Source S be floating potential. Thus, voltage is impressed, energy is given to the electron of the tunneling reason between band-bands by the electric field near the drain, and it pours into charge accumulation layer 4b by the side of a drain field. Charge accumulation layer 4b is located in an electronic direction of grouting by having formed the level difference 26 in the channel field 25. For this reason, the injection efficiency of the electron to charge accumulation layer 4b can improve, and improvement in the speed of grouting velocity and reduction-ization of applied voltage can be attained. the case where an electron is poured into charge accumulation layer 4a by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above-mentioned case On the other hand, as shown in drawing 92 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using Fowler Nordheim (FN) mold tunnel current. Moreover, when the gate electrode 3 is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, what is necessary is just to let Source S and Drain D be the n-type-semiconductor substrate 19 and this potential. Moreover, it is also possible to impress different positive voltage from the potential of the p type semiconductor substrate 1 to Drain D, and to draw out an electron for Source S only from charge accumulation layer 4a by the side of floating potential (Floating), then Drain D. What is necessary is to impress positive voltage to Source S, in drawing out an electron only from charge accumulation layer 4b by the side of Source S, and just to let Drain D be floating potential.

[0142] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.
[0143] Next, the manufacture method of the memory cell of the nonvolatile memory concerning the gestalt of operation of the 10th of this invention is explained using drawing 93 thru/or drawing 101 . As first shown in drawing 93 , the wrap photoresist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19. And as shown in drawing 94 , a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.
[0144] Next, as shown in drawing 95 , the small silicon nitride of charge storage capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method. Silicon oxide is deposited with a CVD method after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
[0145] next, it is shown in drawing 96 -- as -- the n-type-semiconductor substrate 19 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, dry etching of the 1st gate insulator layer 13, the surface 2nd gate insulator layer 14, and the surface 3rd gate insulator layer 15 of the n-type-semiconductor substrate 19 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask is carried out in self align.
[0146] Next, as shown in drawing 97 , the space 17 for charge accumulation layer formation is formed. This space 17 is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 10th of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. Moreover, the space 17 for charge accumulation layer formation may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.
[0147] next, it is shown in drawing 98 -- as -- the n-type-semiconductor substrate 19 whole surface -- LPCVD -- it deposits so that the space 17 for charge accumulation layer formation may be thoroughly embedded by law in the high silicon nitride 18 of charge storage capacity. And as shown in drawing 99 , anisotropic etching by RIE is performed to the n-type-semiconductor substrate 19 whole surface, and the charge accumulation layers 4a and 4b which consisted of high silicon nitrides of charge storage capacity are formed.
[0148] Next, as shown in drawing 100 , after forming an oxide film 16 all over n-type-semiconductor substrate 19, p-mold diffusion layer 20 of low high impurity concentration is formed. It forms by activating the impurity which p-mold diffusion layer 20 used the gate electrode 3 as the mask with ion-implantation technology, poured in p mold impurity, and was poured in by subsequent heat treatment.
[0149] Next, as shown in drawing 101 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, p+ mold diffusion layer 21 of high high impurity concentration is formed. It forms by activating the impurity which p+ mold diffusion layer 21 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in p mold impurity, and was poured in by subsequent heat treatment.
[0150] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere -- the gate electrode 3 and p+ mold diffusion layer 21 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 90 will be completed.
[0151] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 90 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a

passivation film formation process, one by one.
[0152] Thus, with the gestalt of the 10th operation of this invention, the charge accumulation layers 4a and 4b can be formed in the lower part of the ends of the gate electrode 3 in self align. Therefore, detailed-ization of the direction of gate length of a cel transistor is attained. Thereby, large capacity and the non-volatile semiconductor memory of high density can be offered. Moreover, the cel area per bit is mostly reduced by half compared with the former, and non-volatile semiconductor memory reduced substantially can be realized.
[0153] Moreover, the width of face of the direction of channel length of the charge accumulation layers 4a and 4b is easily controllable by accommodation of the etching speed difference of the 1st gate insulator layer 13 and the 3rd gate insulator layer 15, and the 2nd gate insulator layer 14, and etching time. Thereby, the charge accumulation layers 4a and 4b can be arranged to the symmetry. And since the charge accumulation layers 4a and 4b are electrically separated thoroughly by the 2nd gate insulator layer 14, the interaction between charge accumulation layer 14a and 14b does not happen. Furthermore, since the charge accumulation layers 4a and 4b are thoroughly insulated from a source field, a drain field, the gate electrode 3, and a channel field with the 1st insulator layer 13 and the 3rd insulator layer 15, and an oxide film 16, the non-volatile semiconductor memory which was excellent in the charge maintenance property can be offered. It is extended and formed in the direction of a channel field from the edge of the gate electrode 3, and the charge accumulation layers 4a and 4b are current transfer-characteristics ********** of a memory cell by the charge storage condition of the portion by the side of the channel field of the charge accumulation layers 4a and 4b. Therefore, if the gate length lay length of this portion is reduced to a limit, more detailed non-volatile semiconductor memory can be offered.
[0154] Furthermore, since the cellular structure is easily realizable at the usual CMOS process, non-volatile semiconductor memory can be manufactured by low cost using the existing production line.
[0155] And with the gestalt of operation of the 10th of this invention, the electronic injection efficiency at the time of writing can be raised. For this reason, improvement in the speed of drawing speed and reduction-ization of the applied voltage at the time of writing can be attained.
[0156] (Gestalt of the 11th operation) Next, the gestalt of operation of the 11th of this invention is explained. In the gestalt of the 10th operation of the above, the gestalt of operation of the 11th of this invention made unnecessary the 2nd insulator layer 14 arranged between charge accumulation layer 4a of drawing 90 , and charge accumulation layer 4b, and has taken the configuration which made two charge accumulation layers 4a and 4b unify. Drawing 102 is a cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 11th of this invention. As shown in drawing 102 , this memory cell structure is changed to the charge accumulation layers 4a and 4b of the gestalt of the 10th operation of the above, and the 2nd insulator layer 14, and arranges 4f of charge accumulation layers.
[0157] Next, the manufacture method of the memory cell of the nonvolatile memory concerning the gestalt of operation of the 11th of this invention is explained using Fig. 103 thru/or 108 . Like the gestalt of the 10th operation of the above, as first shown in drawing 103 , the wrap photoresist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19. And as shown in drawing 104 , a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.
[0158] Next, as shown in drawing 105 , the small silicon nitride of charge storage capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method. after 1st gate insulator layer 13 formation and LPCVD -- about 5-10nm of high silicon nitrides 18 of charge storage capacity is formed by law. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed.
[0159] next, it is shown in drawing 106 -- as -- the n-type-semiconductor substrate 19 whole surface -- LPCVD -- after depositing the about 50-250nm polycrystalline silicon film which doped n mold or p mold impurity by law, patterning is carried out with exposure technology and etching technology, and the gate electrode 3 is formed. Then, dry etching of the 1st gate insulator layer 13, the surface silicon nitride 18, and the surface 3rd gate insulator layer 15 of the n-type-semiconductor substrate 19 of the field which forms a source field and a drain field by using the gate electrode 3 as a mask is carried out in self align. Here, 4f of charge accumulation layers is formed.
[0160] Next, as shown in drawing 107 , after forming an oxide film 16 all over n-type-semiconductor substrate 19, p-mold diffusion layer 20 of low high impurity concentration is formed. It forms by activating the impurity which p-mold diffusion layer 20 used the gate electrode 3 as the mask with ion-implantation technology, poured in p mold impurity, and was poured in by subsequent heat treatment.
[0161] Next, as shown in drawing 108 , after forming the sidewall spacer 9 in the side attachment wall of the gate

electrode 3, p+ mold diffusion layer 21 of high high impurity concentration is formed. It forms by activating the impurity which p+ mold diffusion layer 21 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-implantation technology, poured in p mold impurity, and was poured in by subsequent heat treatment.
[0162] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere -- the gate electrode 3 and p+ mold diffusion layer 21 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 102 will be completed.
[0163] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 102 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.
[0164] (Gestalt of the 12th operation) Next, the gestalt of operation of the 12th of this invention is explained. Drawing 109 is a cross section showing the structure of the memory cell of the non-volatile semiconductor memory concerning the gestalt of operation of the 12th of this invention. Although exposure technology and etching technology were used for patterning of the gate electrode 3 with the gestalt of the 10th operation of the above, it is the example which uses the chemical mechanical grinding method for patterning of the gate electrode 3 with the gestalt of this 12th operation.
[0165] Next, the manufacture method of the memory cell of the nonvolatile memory concerning the gestalt of operation of the 12th of this invention is explained using Fig. 110 thru/or 118 . As first shown in drawing 110 , the wrap photoresist pattern 27 is formed except the field in which the channel field 25 is formed on the n-type-semiconductor substrate 19. And as shown in drawing 111 , a level difference 26 is formed by etching the n-type-semiconductor substrate 19 by the RIE method.
[0166] Next, as shown in drawing 112 , the small silicon nitride of charge storage capacity is deposited all over n-type-semiconductor substrate 19, and the about 10nm 1st gate insulator layer 13 is formed. Deposition of the small silicon nitride of charge storage capacity is performed for example, by the JVD method. Silicon oxide is deposited with a CVD method after 1st gate insulator layer 13 formation, and the about 5-10nm 2nd gate insulator layer 14 is formed. Then, the small silicon nitride of charge storage capacity is deposited by the JVD method, and the about 10nm 3rd gate insulator layer 15 is formed. furthermore, the n-type-semiconductor substrate 19 whole surface -- LPCVD -- the about 50-500nm polycrystalline silicon film 28 which doped n mold or p mold impurity by law is deposited.
[0167] Next, as shown in drawing 113 , the gate electrode 3 is formed by performing embedding of the polycrystalline silicon film 19 by the chemical mechanical polishing method. In addition, wet etching usually removes the 1st gate insulator layer 13, the 2nd gate insulator layer 14, and the 3rd gate insulator layer 15 which remain on the n-type-semiconductor substrate 19.
[0168] Next, as shown in drawing 114 , the space 17 for charge accumulation layer formation is formed. This space 17 is formed by carrying out wet etching of the edge of the 2nd gate insulator layer 14 selectively using an etching reagent with the larger etch rate of the 2nd gate insulator layer 14 than the 1st gate oxide 13 and the 3rd gate insulator layer 15. What is necessary is just to use for example, a fluoric acid system as an etching reagent with the gestalt of operation of the 12th of this invention, since the 1st gate oxide 13 and the 3rd gate insulator layer 15 are constituted from a silicon nitride and the 2nd gate insulator layer 14 is constituted from silicon oxide. Moreover, the space 17 for charge accumulation layer formation may be formed by the plasma dry etching method using the gas which changes to the wet etching method which used the etching reagent, and contains HF gas.
[0169] next, it is shown in drawing 115 -- as -- the n-type-semiconductor substrate 19 whole surface -- LPCVD -- it deposits so that the space 17 for charge accumulation layer formation may be thoroughly embedded by law in the high silicon nitride 18 of charge storage capacity. And as shown in drawing 116 , anisotropic etching by RIE is performed to the n-type-semiconductor substrate 19 whole surface, and the charge accumulation layers 4a and 4b which consisted of high silicon nitrides of charge storage capacity are formed.
[0170] Next, as shown in drawing 117 , after forming an oxide film 16 all over n-type-semiconductor substrate 19, p-mold diffusion layer 20 of low high impurity concentration is formed. It forms by activating the impurity which p-mold diffusion layer 20 used the gate electrode 3 as the mask with ion-implantation technology, poured in p mold impurity, and was poured in by subsequent heat treatment.
[0171] Next, as shown in drawing 118 , after forming the sidewall spacer 9 in the side attachment wall of the gate electrode 3, p+ mold diffusion layer 21 of high high impurity concentration is formed. It forms by activating the impurity which p+ mold diffusion layer 21 used the gate electrode 3 and the sidewall spacer 9 as the mask with ion-

implantation technology, poured in p mold impurity, and was poured in by subsequent heat treatment.
[0172] next, the thing for which refractory metal films, such as a tungsten, titanium, and cobalt, are deposited by the CVD method or the spatter all over the n-type-semiconductor substrate 19, then the n-type-semiconductor substrate 19 is heat-treated in an inert atmosphere -- the gate electrode 3 and p+ mold diffusion layer 21 -- the conductive layer 12 which consists of refractory metal silicide is formed in each front face. After conductive layer 12 formation, if the unreacted refractory metal which remained in fields other than the above is removed, the memory cell structure shown in drawing 109 will be completed.
[0173] In addition, although a graphic display is not carried out, a final non-volatile memory cell is completed after memory cell structure completion of drawing 109 through the usual CMOS manufacturing processes, such as an interlayer insulation film formation process, a contact hole formation process, a wiring formation process, and a passivation film formation process, one by one.
[0174] (Gestalt of the 13th operation) Next, the gestalt of operation of the 13th of this invention is explained. With the gestalt of the above-mentioned 1st thru/or the 12th operation, sufficient examination to improvement in the speed of transistors other than a memory cell was not made. On the other hand, as structure of a high-speed CMOS transistor, by forming the notch on concave between a gate electrode and a source drain diffusion layer, the capacity between a gate electrode and a diffusion layer is reduced, and the attempt which accelerates a logic gate is made (T.Ghani et al., IEDM99, p415). The gestalt of this 13th operation is using this structure for non-volatile semiconductor memory, and enables large improvement in the speed of the semiconductor device consolidated with the usual transistor and the non-volatile semiconductor memory which does not have a memory function.
[0175] Drawing 119 is a cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 13th of this invention. This memory cell consists of n mold MOS transistors. With the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 13th of this invention, the gate electrode 3 is formed in the front face of the p type semiconductor substrate 1 through the 1st gate insulator layer 13. A crevice is established in the ends of the gate electrode 3, and the charge accumulation layer 4 (4a, 4b) is formed in each crevice. The oxide film 30 is formed between the charge accumulation layer 4 and the gate electrode 3. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of this sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.
[0176] The memory cell of the nonvolatile memory concerning the gestalt of operation of the 13th of this invention has the LDD structure which constituted the source field and the drain field from an n-mold diffusion layer 10 of low high impurity concentration, and an n+ mold diffusion layer 11 of high high impurity concentration. And the charge accumulation layer 4 (4a, 4b) is formed in the both ends of the gate electrode 3. An electron is accumulated in these two charge accumulation layers 4a and 4b. That are recording condition (1) charge accumulation layer 4a, All of 4b can take the condition which is not accumulating the electron, the condition that only (2) charge accumulation layer 4a is accumulating the electron, the condition that only (3) charge accumulation layer 4b is accumulating the electron, and four conditions of condition ** that (4) charge accumulation layers 4a and 4b are accumulating the electron. A changed part of the threshold voltage produced by the existence of the electron held in these two charge accumulation layers 4a and 4b is made to correspond to "00" of storage information, "01", "10", and "11." Moreover, with this memory cell structure, since the charge accumulation layer 4 is located above the channel field edge, the threshold voltage of a channel field center section is decided only by high impurity concentration of a channel field, and it does not depend for it on the are recording condition of the electron of the charge accumulation layer 4. Therefore, fault elimination (over-erase) by the excess and deficiency of the electron of the charge accumulation layer 4 is prevented, and cannot produce the poor leak which originates in fault elimination by that cause, a poor program, and poor read-out. Moreover, the leakage current between a source field and a drain field can be controlled only with gate voltage, and can realize highly reliable nonvolatile memory. What is necessary is for the charge accumulation layer 4 just to consist of high silicon nitrides of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply. Furthermore, if the 1st gate insulator layer 13 is constituted from a silicon nitride (Si3N4 film) which has an about 2 times [of silicon oxide (SiO2 film)] dielectric constant, silicon oxide conversion thickness can stabilize for it and realize the very thin gate insulator layer which is 4nm - about 11nm. For example, since the real thickness of the silicon nitride whose silicon oxide conversion thickness is 5nm is about 10nm,

induction of the direct tunnel (DT) impregnation is not carried out. Therefore, voltage at the time of electronic impregnation extract actuation is low-battery-ized, and not only detailed-izing of a memory cell but detailed-ization of a circumference high-tension actuation element of it is attained.

[0177] Although n-mold diffusion layer 10 is established for the object of the improvement in resisting pressure of a source field and a drain field and LDD structure is constituted from a memory cell of the nonvolatile memory concerning the gestalt of operation of the 13th of this invention, a source field and a drain field may consist of single drain structure and double drain structure.

[0178] Next, actuation of the nonvolatile memory concerning the gestalt of operation of the 13th of this invention is explained using Fig. 120 and 121 . Drawing 120 is a cross section of the nonvolatile memory explaining write-in actuation. Drawing 121 is a cross section of the nonvolatile memory explaining elimination actuation. The memory cell of Fig. 120 and 121 consists of n mold MOS transistors. As shown in drawing 120 , at the time of the writing of a memory cell, about 6-8V is impressed to Gate G, about 4-5V is impressed to Drain D, respectively, and Source S is grounded. Thus, voltage is impressed and an electron is poured into charge accumulation layer 4b by the side of a drain field with a channel thermoelectron (CHE). the case where an electron is poured into charge accumulation layer 4b by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above On the other hand, as shown in drawing 121 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using Fowler Nordheim (FN) mold tunnel current. Moreover, when Gate G is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, what is necessary is just to let Source S and Drain D be the p type semiconductor substrate 1 and this potential. Moreover, it is also possible to impress different positive voltage from the potential of the p type semiconductor substrate 1 to a drain electrode, and to draw out an electron for a source electrode only from charge accumulation layer 4b by the side of floating potential (Floating), then a drain electrode. What is necessary is to impress positive voltage to a source electrode, in drawing out an electron only from charge accumulation layer 4a by the side of a source electrode, and just to let a drain electrode be floating potential.

[0179] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0180] Next, the actuation of the nonvolatile memory concerning the gestalt of operation of the 13th of this invention which consists of p mold MOS transistors is explained using Fig. 122 and 123 . Drawing 122 is a cross section of the nonvolatile memory explaining write-in actuation. Drawing 123 is a cross section of the nonvolatile memory explaining elimination actuation. The memory cell of Fig. 122 and 123 consists of p mold MOS transistors. As shown in drawing 122 , at the time of the writing of a memory cell, about 5V is impressed to Gate G, and about -5V is impressed to Drain D, respectively, and let Source S be floating potential. Thus, voltage is impressed, energy is given to the electron of the tunneling reason between band-bands by the electric field near the drain field, and an electron is poured into charge accumulation layer 4b by the side of a drain field. the case where an electron is poured into charge accumulation layer 4a by the side of a source field -- Drain D and Source S -- what is necessary is to be alike, respectively and just to replace the voltage to impress with the above On the other hand, as shown in drawing 123 , elimination of a memory cell impresses negative voltage (- -5 V) to Gate G, and is performed by drawing out an electron from the charge accumulation layers 4a and 4b using FN current. Moreover, when Gate G is shared by two or more memory cells, an electron can be simultaneously drawn out from those memory cells. In this case, let Source S and Drain D be the n-type-semiconductor substrate 19, this potential, or floating potential.

[0181] Moreover, although a graphic display is not carried out, read-out of a memory cell is performed by detecting the read-out current which flows between Source S and Drains D. It uses that the current transfer characteristics a source field and near the drain field (channel conductance) become irregular according to the are recording condition of the charge accumulation layers 4a and 4b. To which bias shall be carried out between Source S and Drain D should just choose the direction where the modulation of current transfer characteristics appears notably. According to four are recording conditions of the charge accumulation layers 4a and 4b, four different current transfer characteristics are acquired and, thereby, the information for 2 bits can be memorized in one cel.

[0182] With the gestalt of operation of the 13th of this invention, as shown in drawing 124 , the usual MOS transistor

which does not have a memory function is also realizable. Because, in this MOS transistor, the charge accumulation layer 4 is arranged only on the source drain field 10 and 11, and is not arranged on the channel field. For this reason, the conduction property of this MOS transistor is because effect is not received in the maintenance condition of the charge of the charge accumulation layer 4 at all. Furthermore, by existence of the crevice of the gate electrode 3, the parasitic capacitance between gate-source drains is reduced and it also has the advantageous point that the high-speed operation of an MOS transistor becomes possible.

[0183] (Gestalt of the 14th operation) Next, the gestalt of operation of the 14th of this invention is explained. The gestalt of this 14th operation has the composition of having made the charge accumulation layer 4 and the sidewall spacer 9 unifying, in the gestalt of the 13th operation of the above. Drawing 125 is a cross section showing the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 14th of this invention. This memory cell consists of n mold MOS transistors. With the memory cell structure of the non-volatile semiconductor memory concerning the gestalt of operation of the 14th of this invention, the gate electrode 3 is formed in the front face of the p type semiconductor substrate 1 through the 1st gate insulator layer 13. A crevice is established in the ends of the gate electrode 3, and the charge accumulation layer 4 (4a, 4b) is formed in each crevice. The oxide film 30 is formed between the charge accumulation layer 4 and the gate electrode 3. The sidewall spacer 9 is formed in the side of the gate electrode 3 through an oxide film 16, and a part of this sidewall spacer 9 constitutes the charge accumulation layer 4. n-mold diffusion layer 10 of the low high impurity concentration which touches a channel field, and n+ mold diffusion layer 11 of the high high impurity concentration located in the outside of this n-mold diffusion layer 10 are formed in the principal plane of the p type semiconductor substrate 1 of the lower part of the sidewall spacer 9. the gate electrode 3 and n+ mold diffusion layer 11 -- a conductive layer 12 is formed in each front face.

[0184] What is necessary is for the gestalt of operation of the 14th of this invention just to constitute the sidewall spacer 9 and the charge accumulation layer 4 from the high silicon nitride of the charge storage capacity by the CVD method. It is because the charge maintenance property of being hard to receive effect in the membraneous quality of a lower insulator layer can be acquired by accumulating an electron in the discrete charge trapping level of a silicon nitride. Moreover, if constituted from a silicon film and a polycrystalline silicon film, it can manufacture cheaply.

[0185] With the gestalt of operation of the 14th of this invention, the usual MOS transistor as shown in drawing 126 as well as the gestalt of the 13th operation of the above is realizable.

[0186]

[Effect of the Invention] According to this invention, the structure of a non-volatile semiconductor memory where the information for two or more bits is memorizable by the easy cellular structure is realizable.

[0187] According to this invention, the manufacture method of a non-volatile semiconductor memory of manufacturing the non-volatile semiconductor memory which memorizes the information for two or more bits in an easy manufacture process is realizable.

[0188] According to this invention, the structure of the semiconductor memory which wrote in electrically by the easy cellular structure and loaded together eliminable nonvolatile memory and the volatile memory in which read-out write-in [high-speed] is possible is realizable.

[0189] According to this invention, the manufacture method of the semiconductor memory which wrote in electrically in the easy manufacture process and loaded together eliminable nonvolatile memory and the volatile memory in which read-out write-in [high-speed] is possible is realizable.

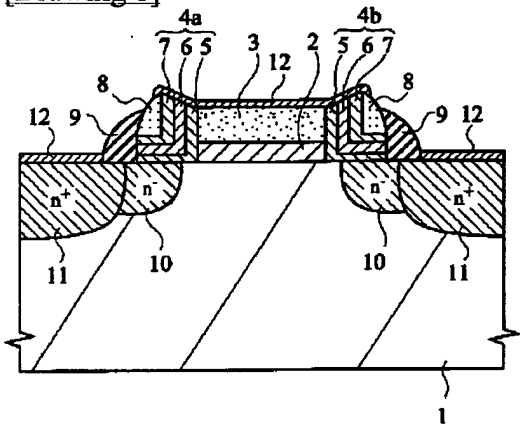
[Translation done.]

* NOTICES *

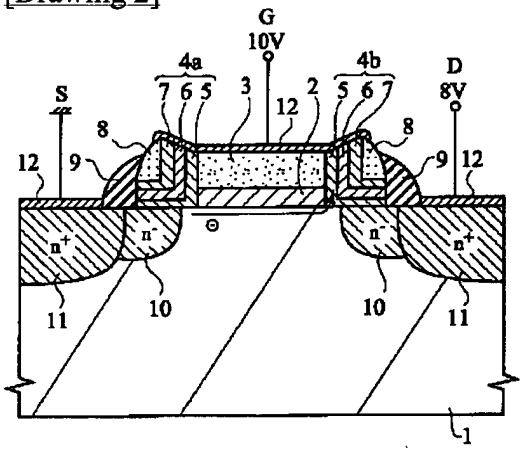
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

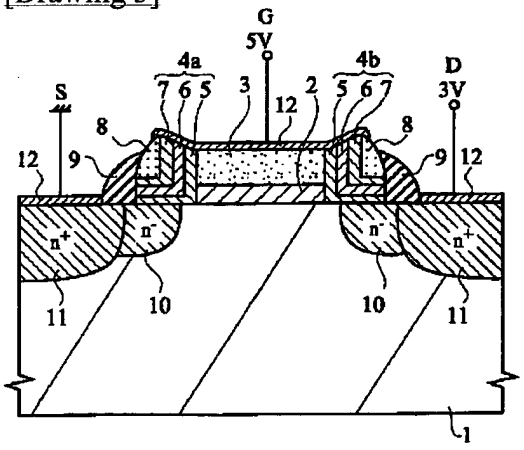
[Drawing 1]



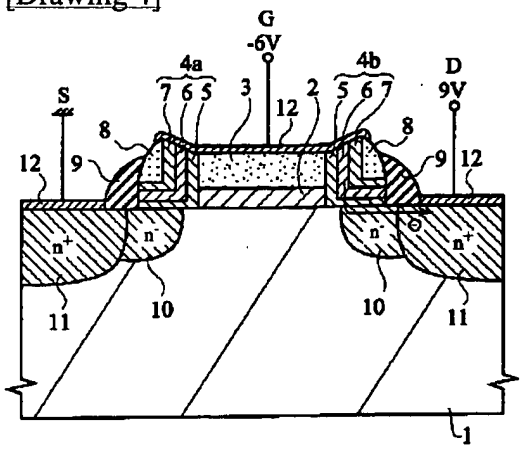
[Drawing 2]



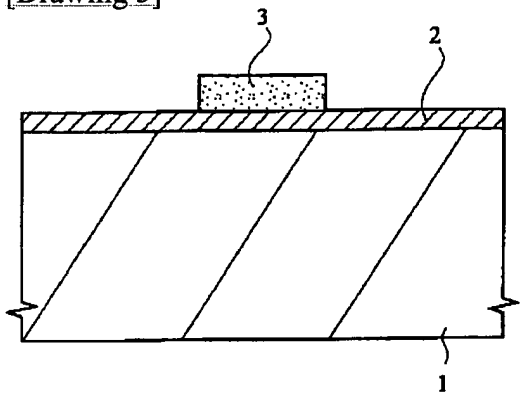
[Drawing 3]



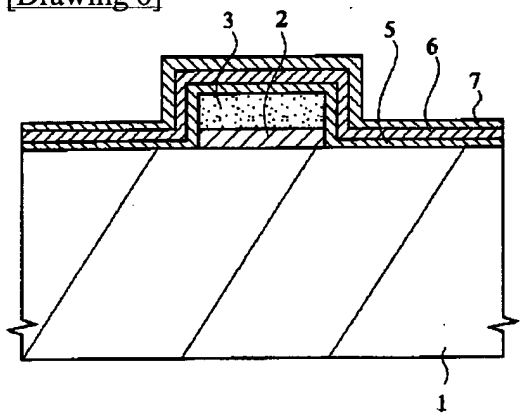
[Drawing 4]



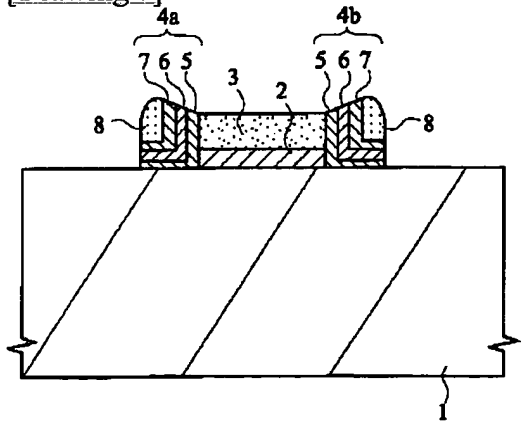
[Drawing 5]



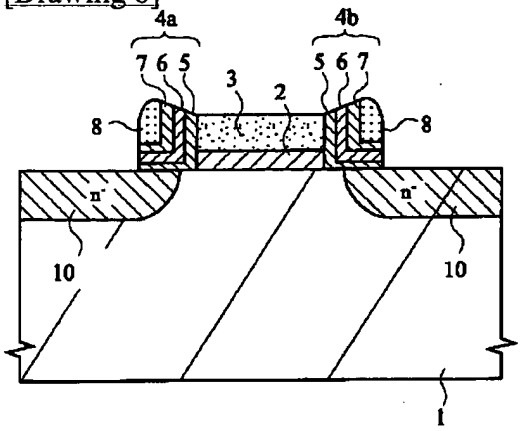
[Drawing 6]



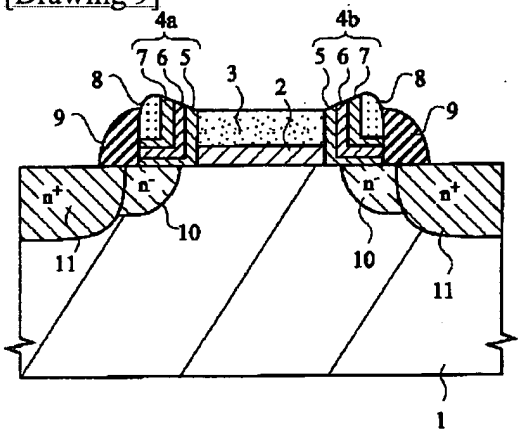
[Drawing 7]



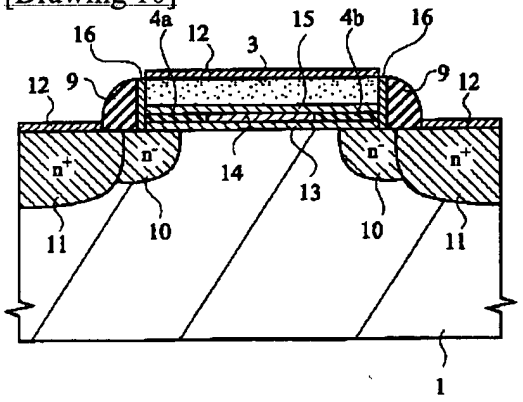
[Drawing 8]



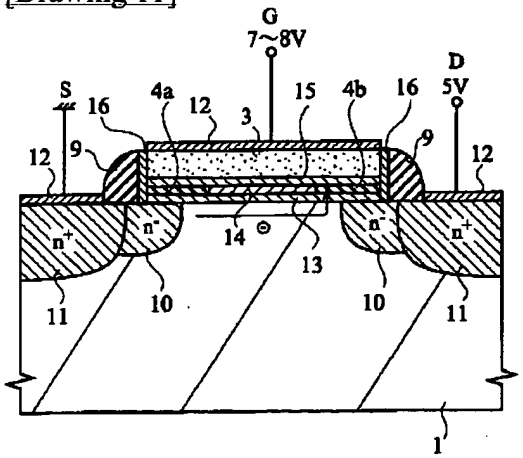
[Drawing 9]



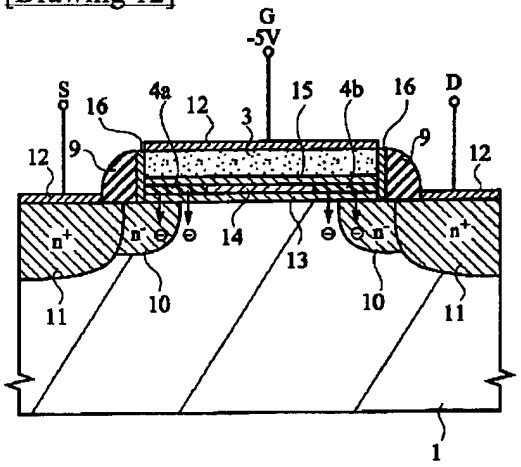
[Drawing 10]



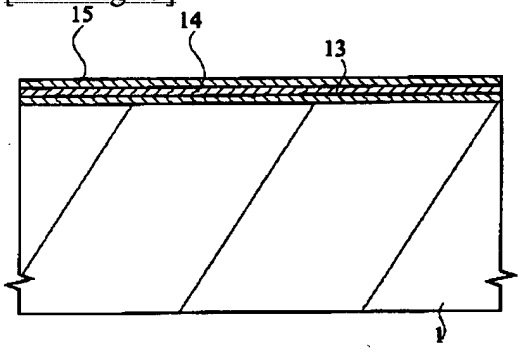
[Drawing 11]



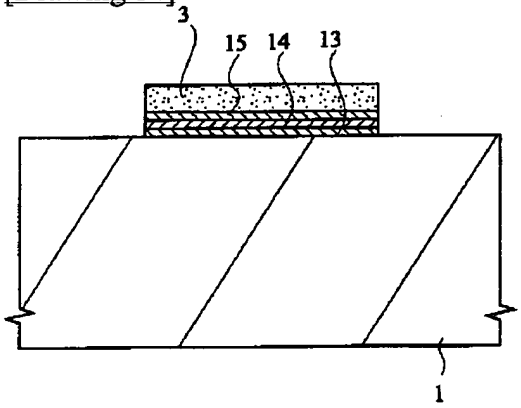
[Drawing 12]



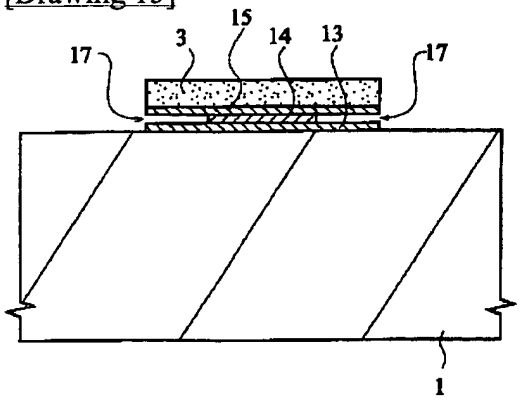
[Drawing 13]



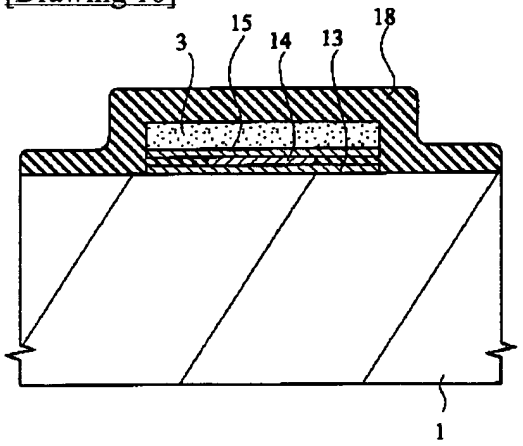
[Drawing 14]



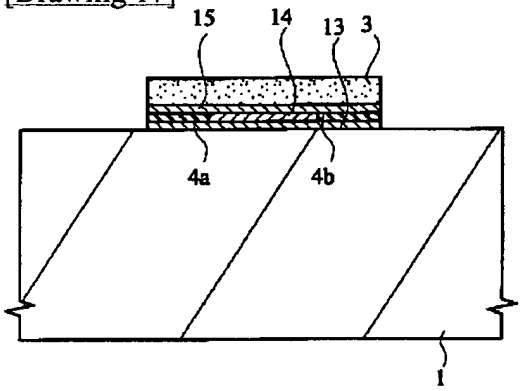
[Drawing 15]



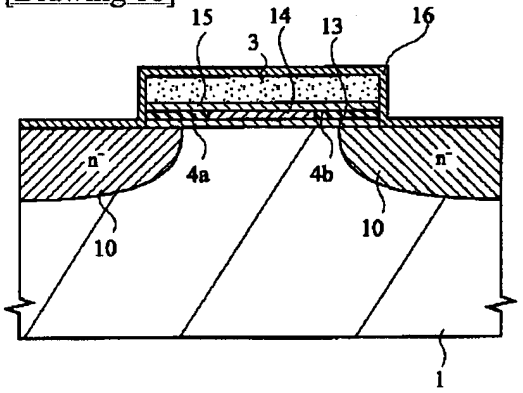
[Drawing 16]



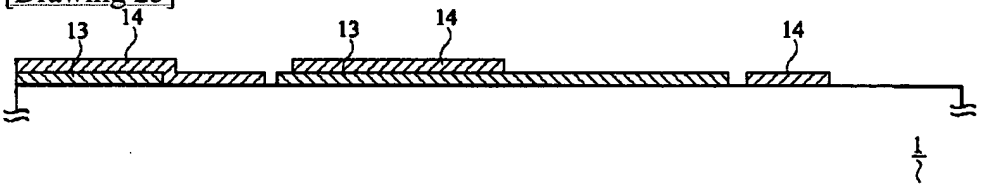
[Drawing 17]



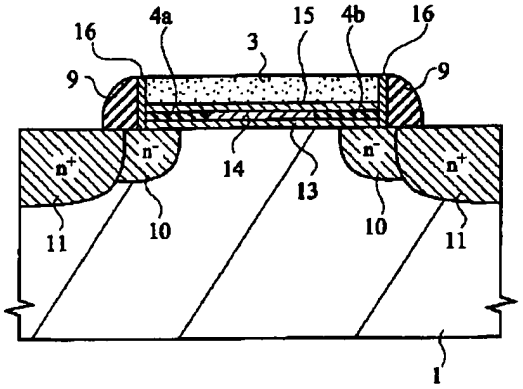
[Drawing 18]



[Drawing 25]



[Drawing 19]



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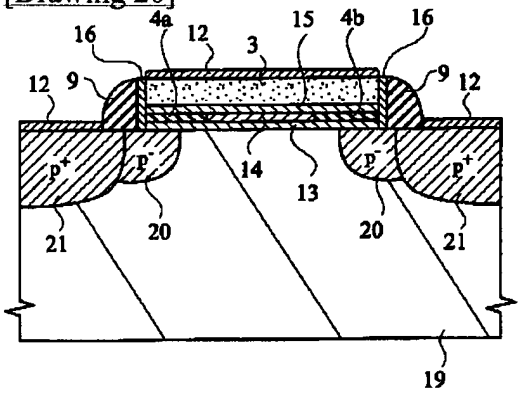

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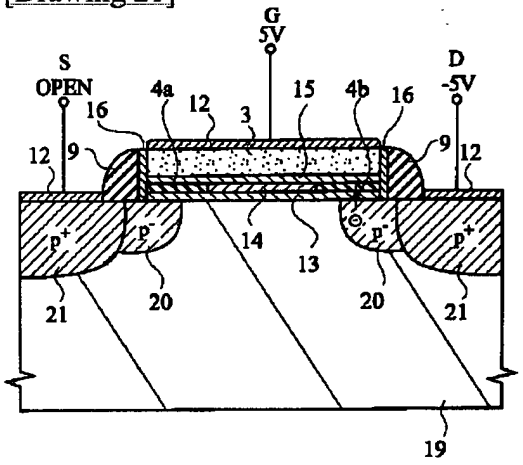

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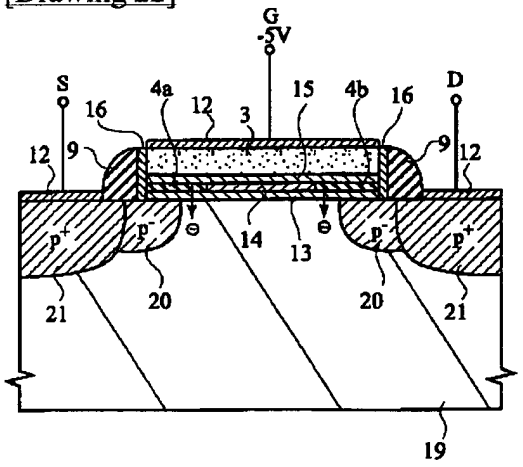

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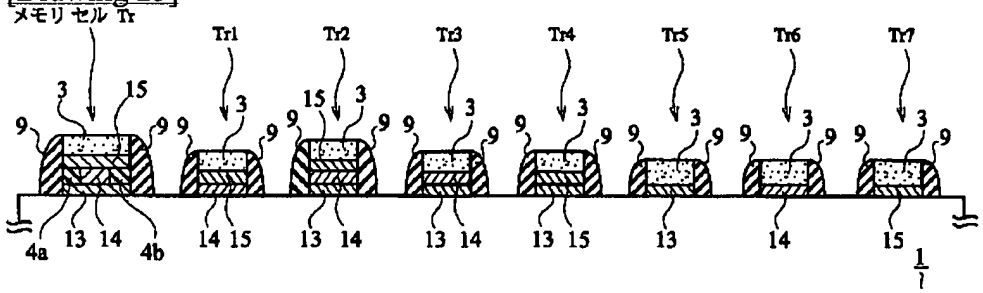

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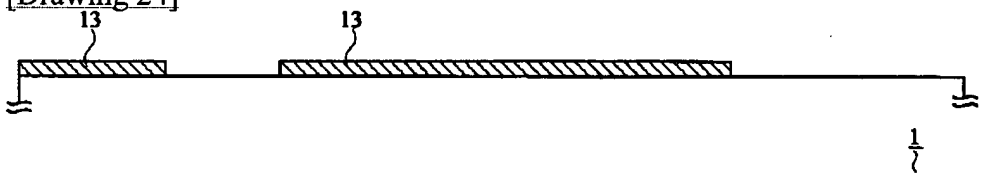

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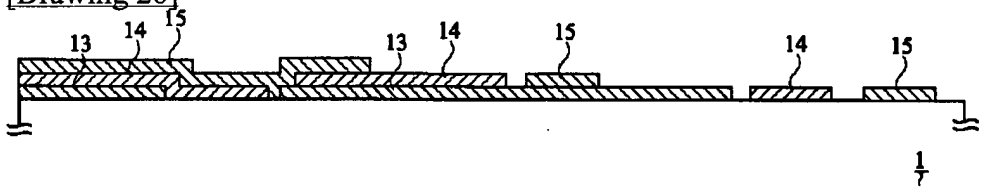

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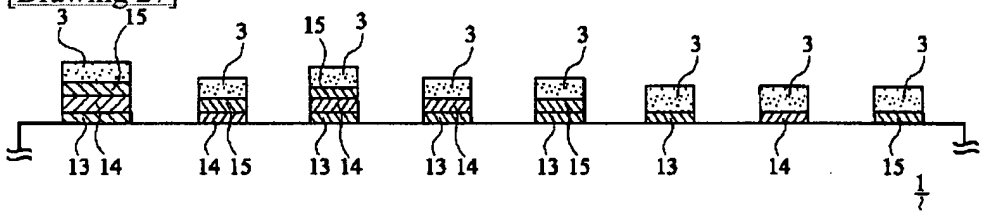

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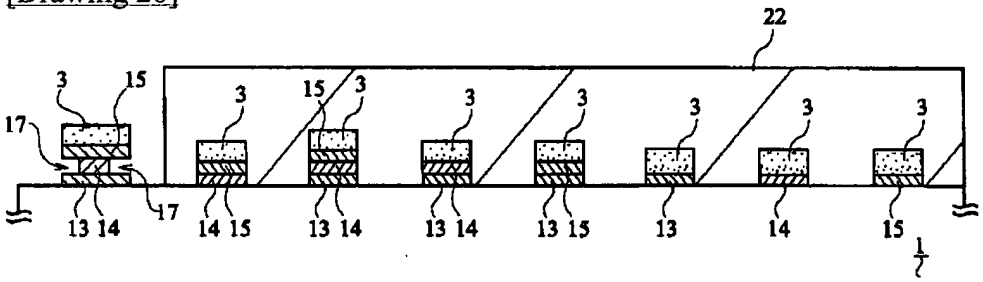

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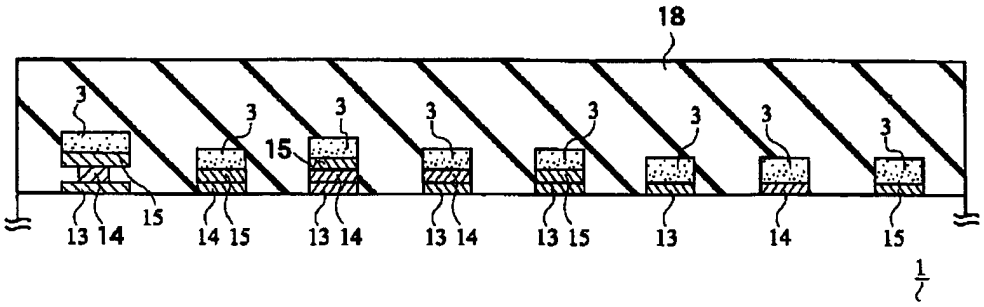

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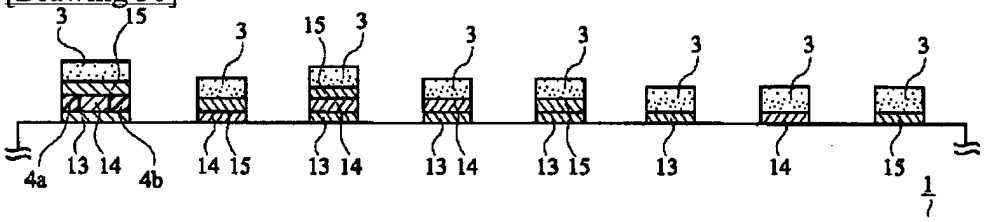

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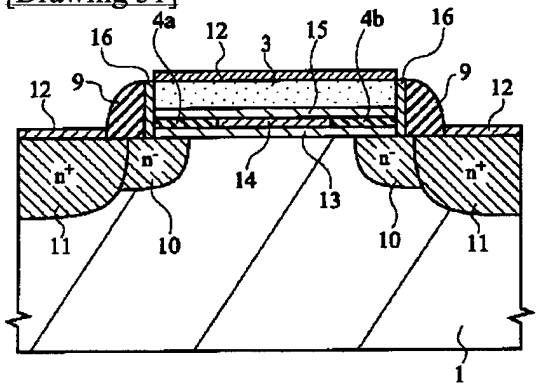

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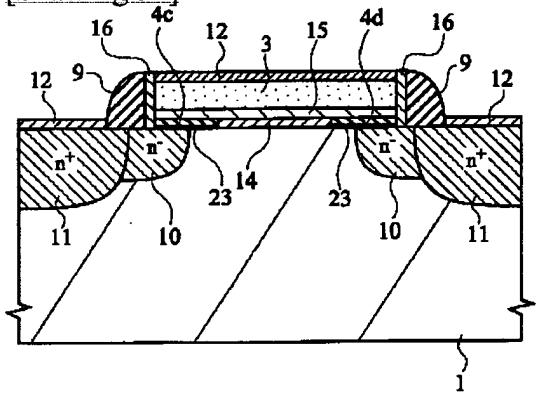

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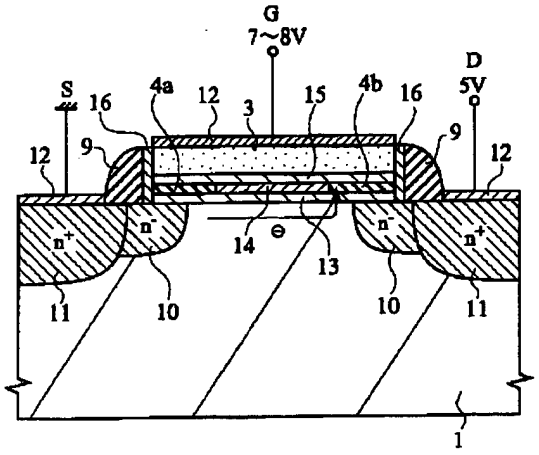

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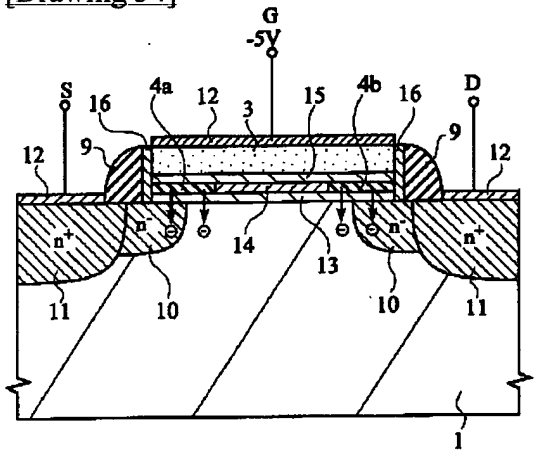

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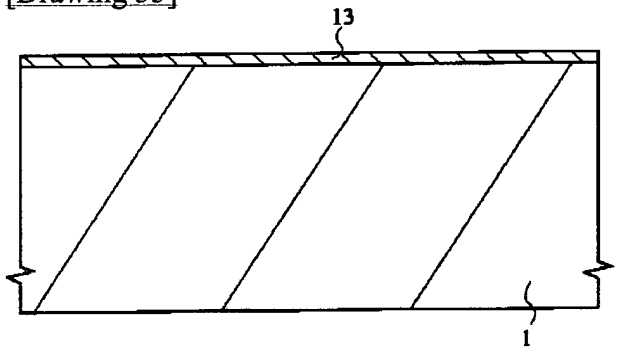

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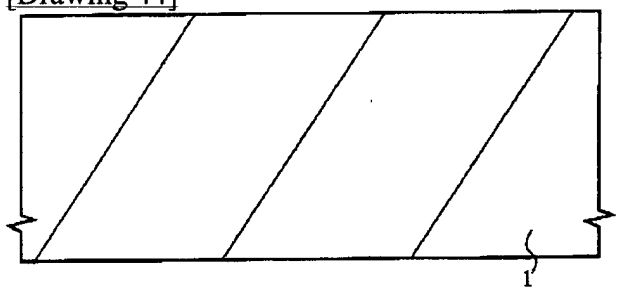

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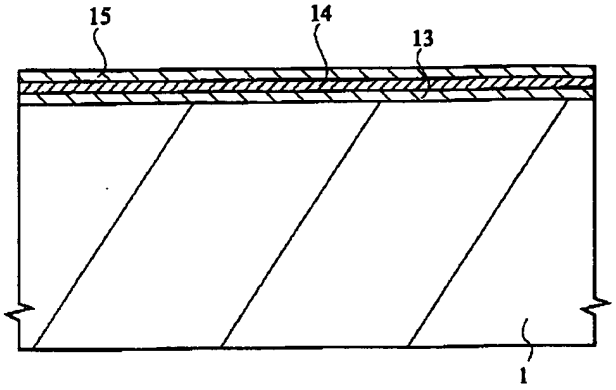

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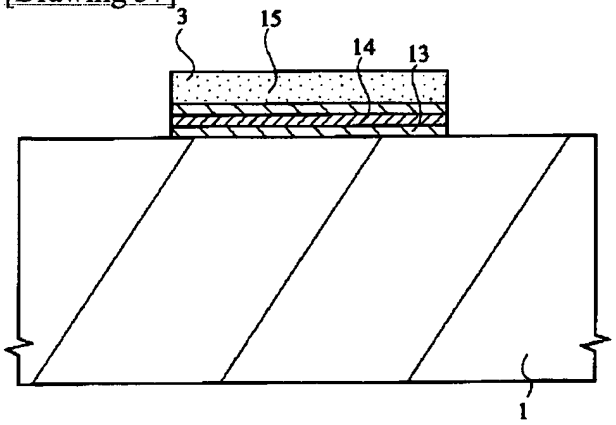

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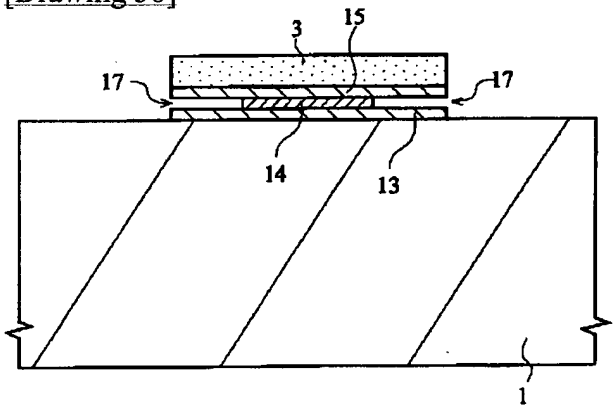

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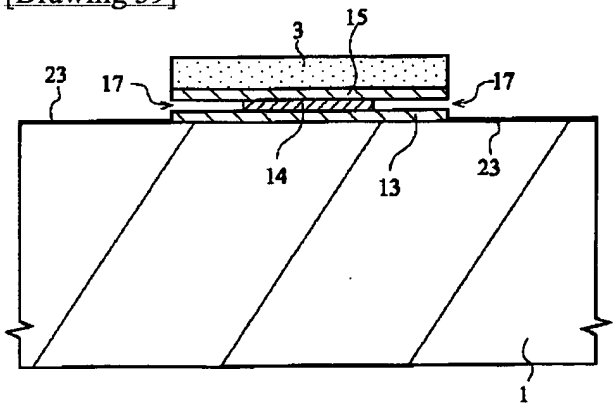

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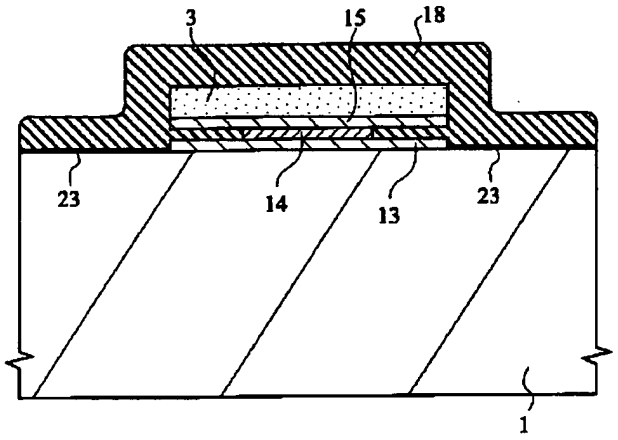

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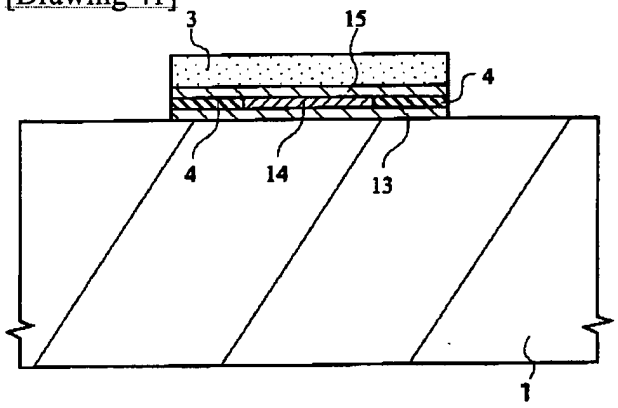

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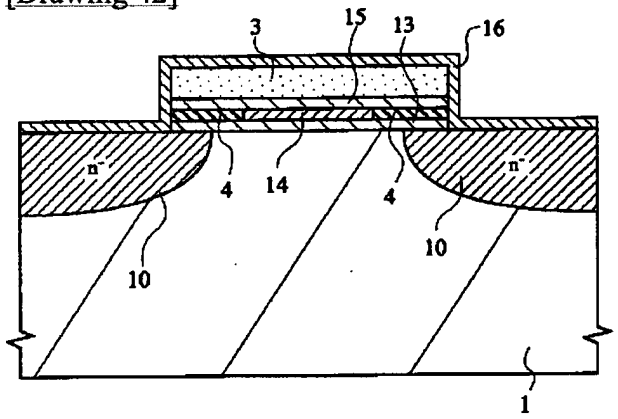

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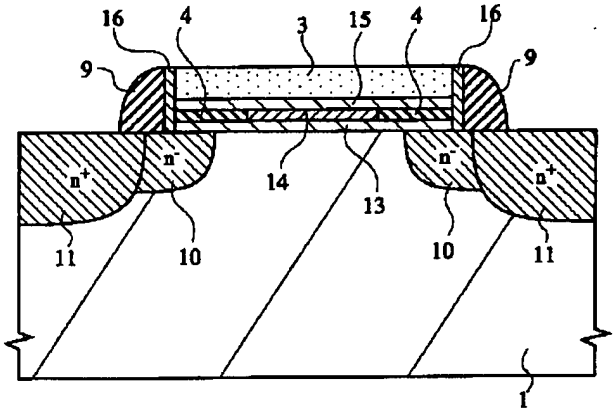

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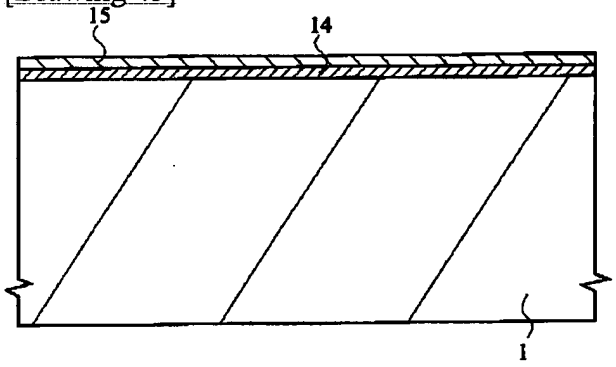

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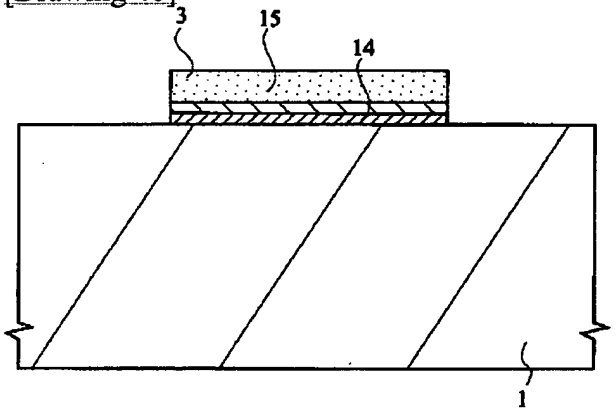

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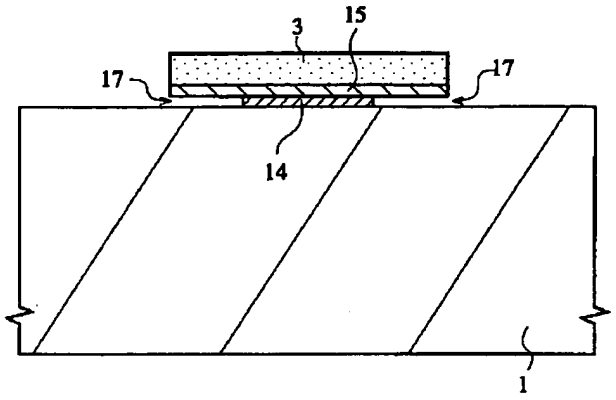

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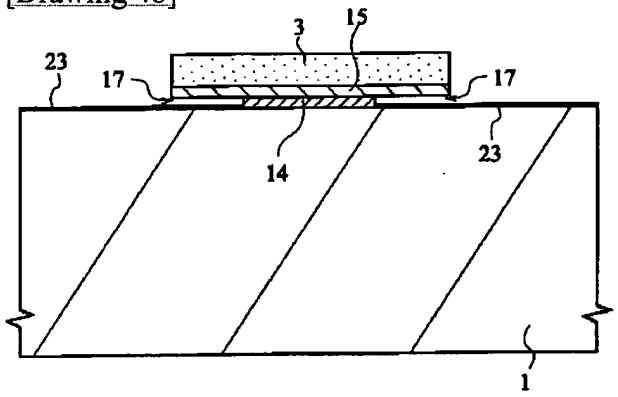

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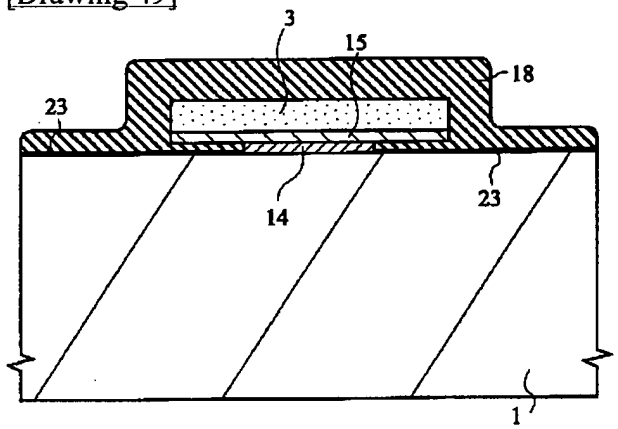

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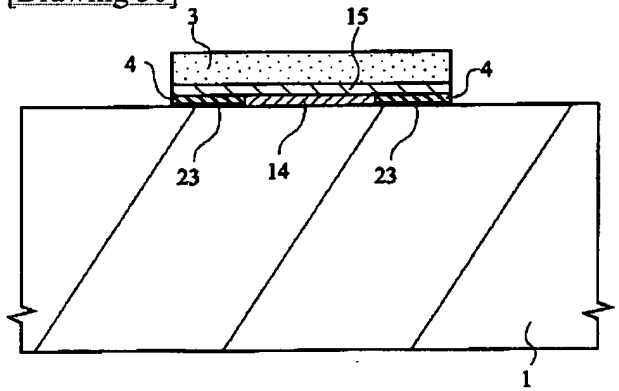

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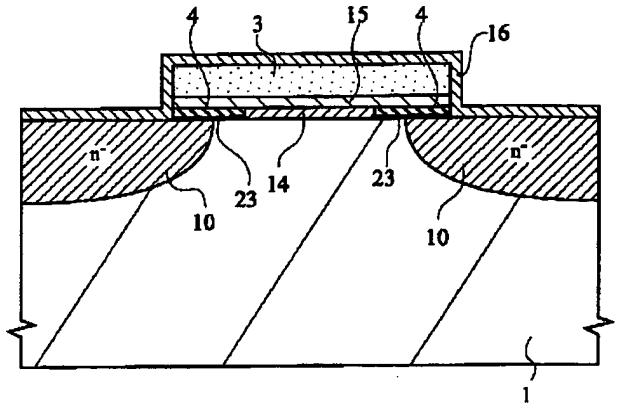

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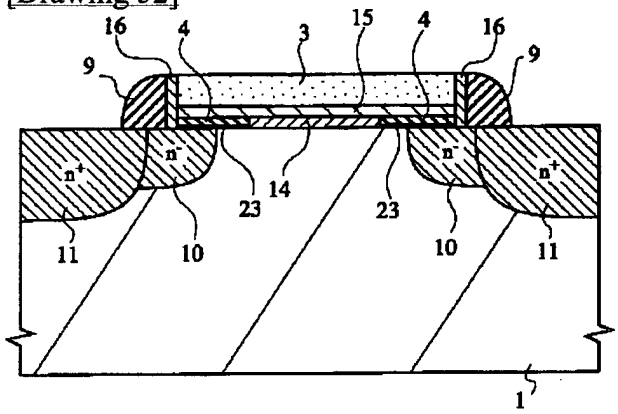

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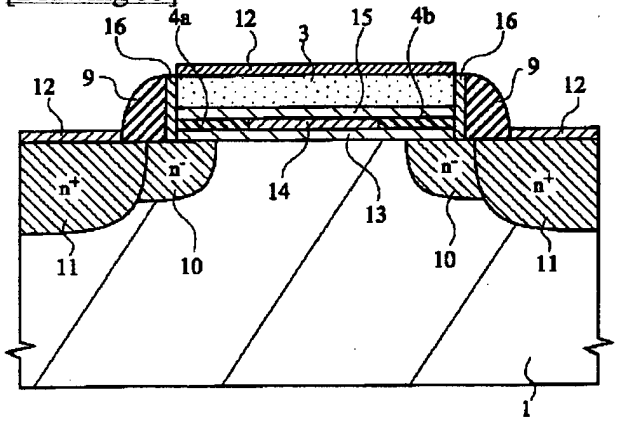

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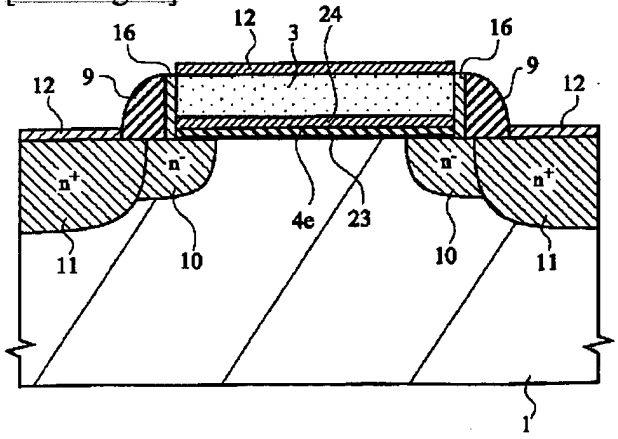

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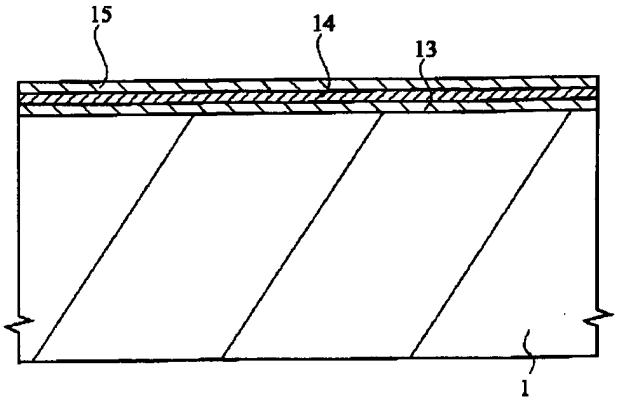

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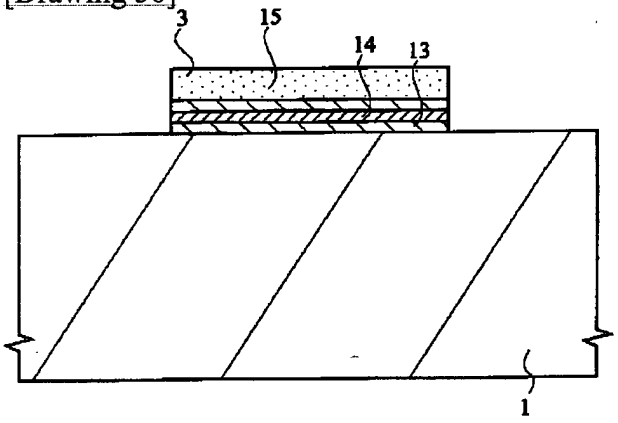

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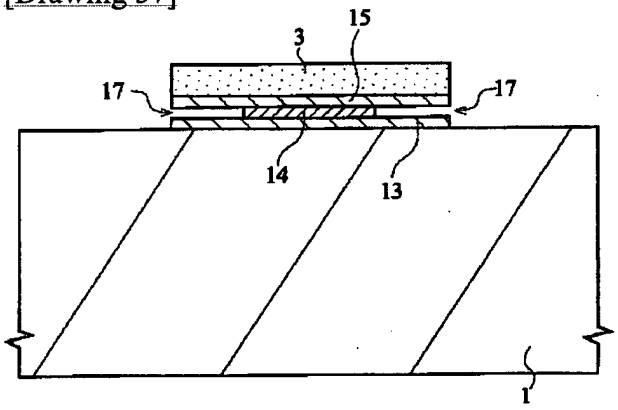

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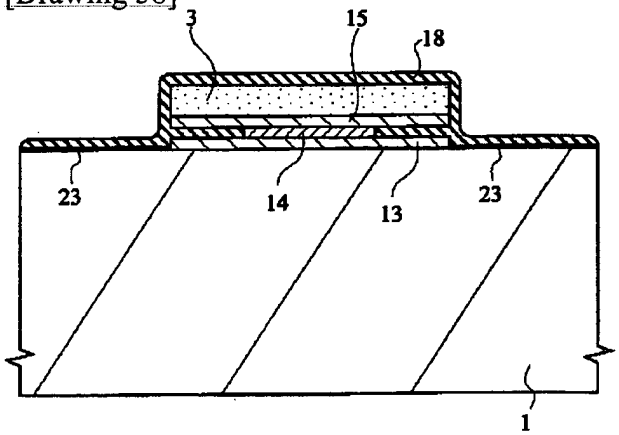

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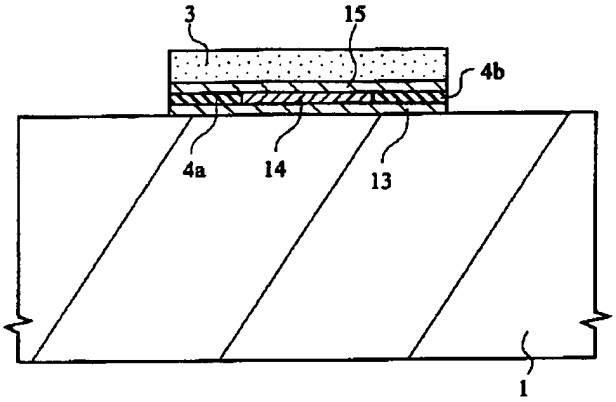

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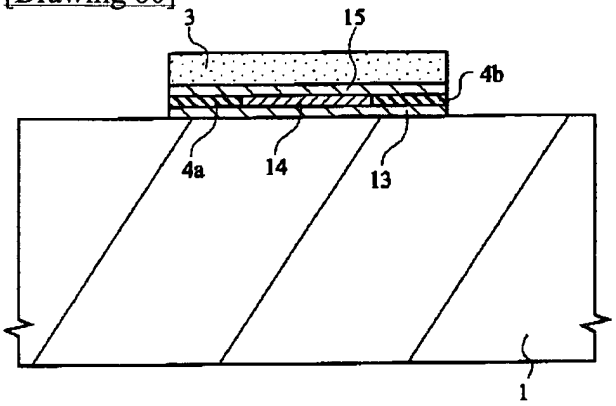

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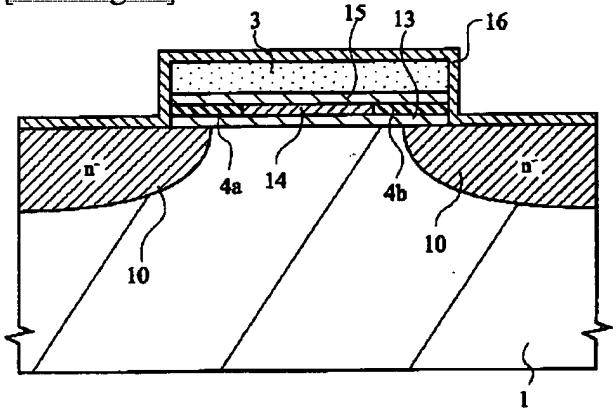

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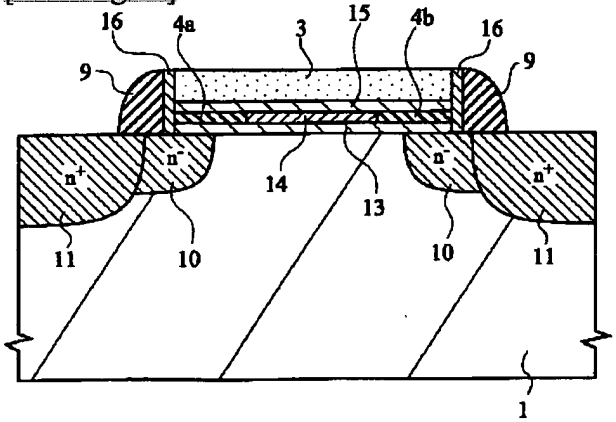

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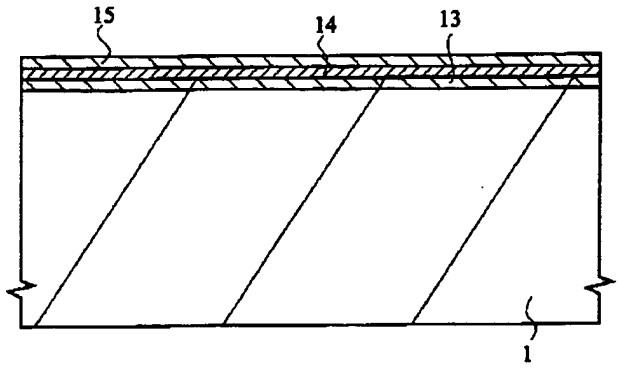

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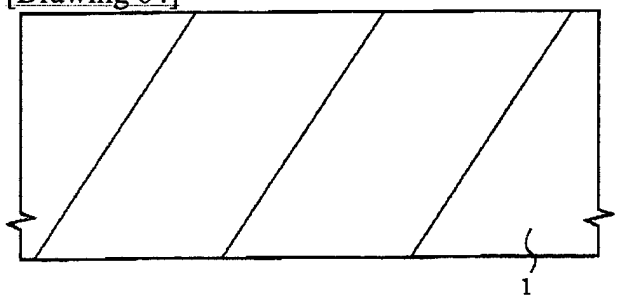

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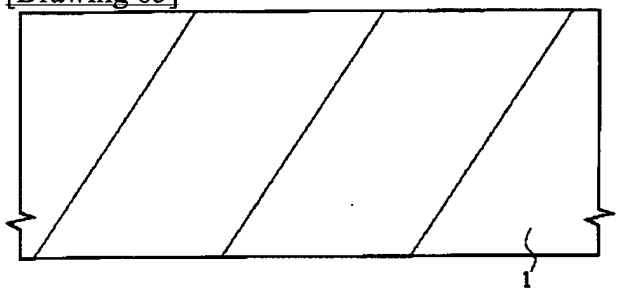

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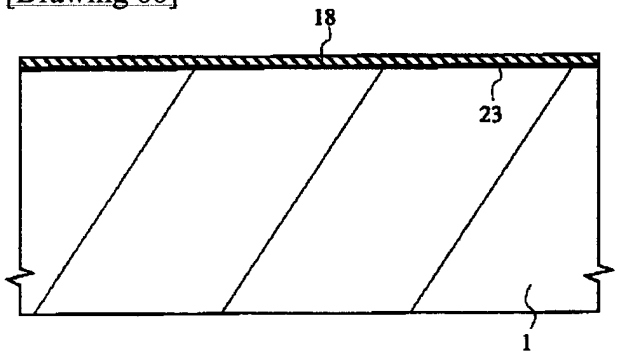

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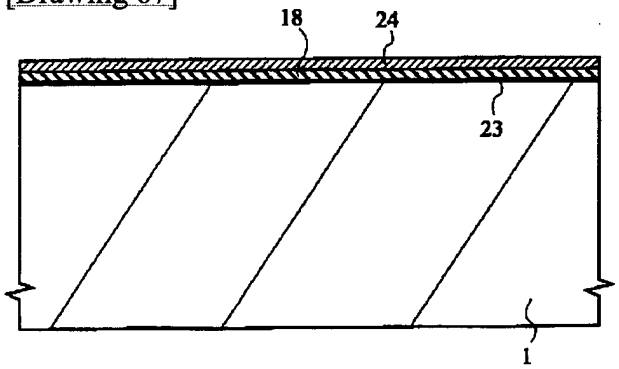

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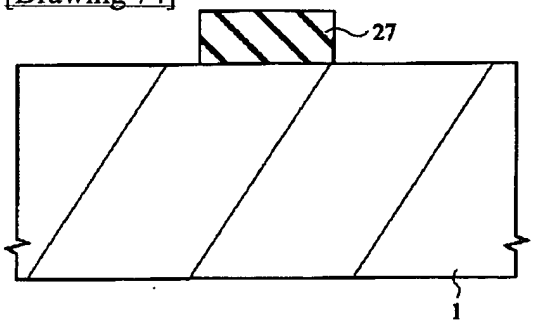

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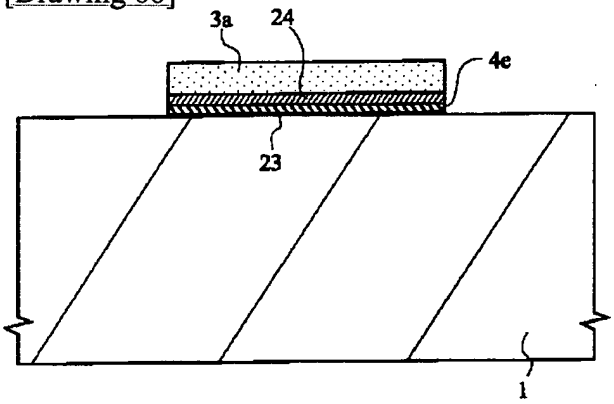

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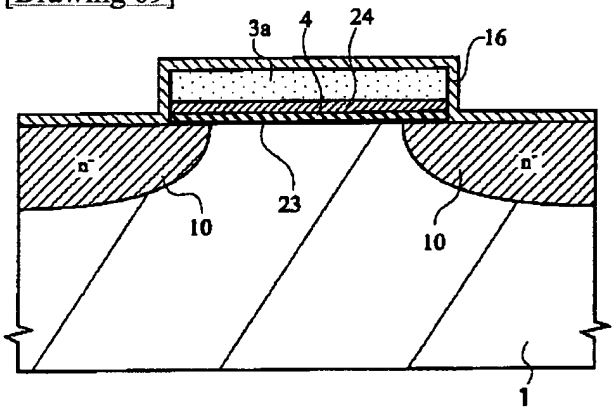

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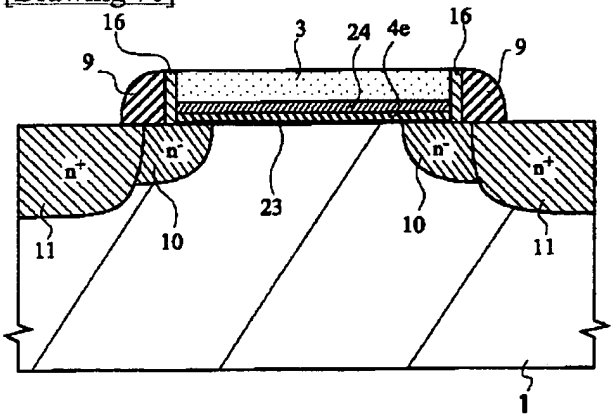

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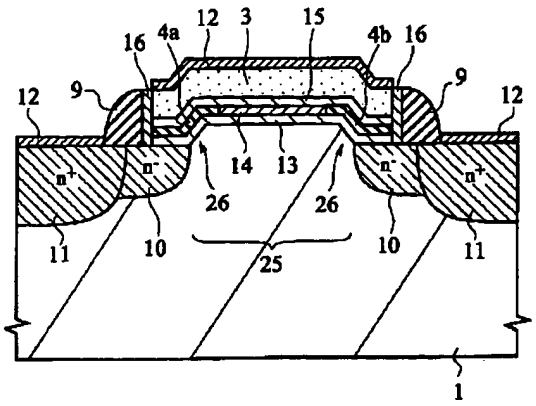

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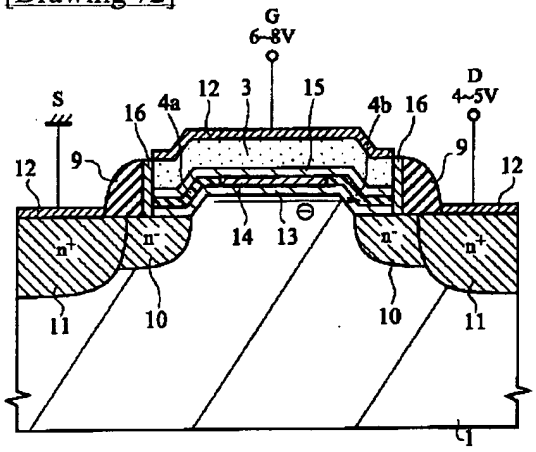

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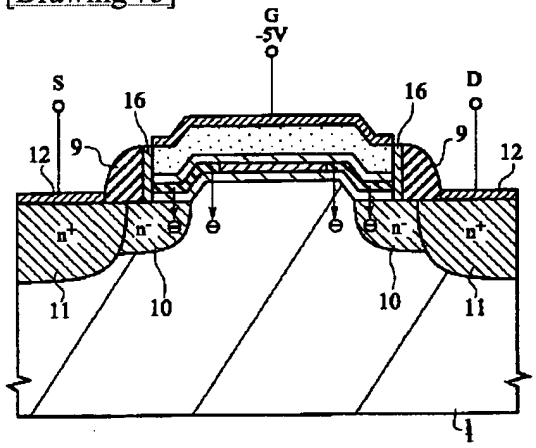

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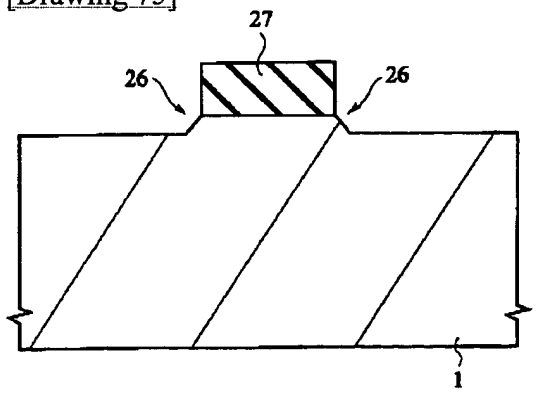

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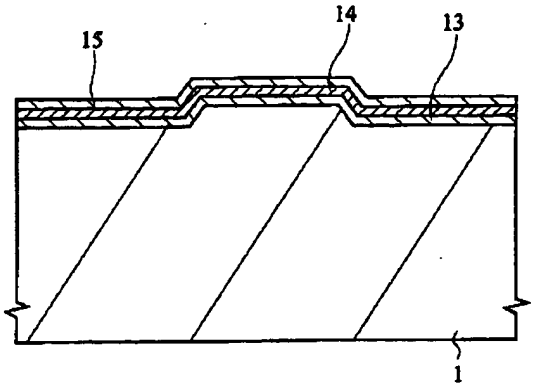

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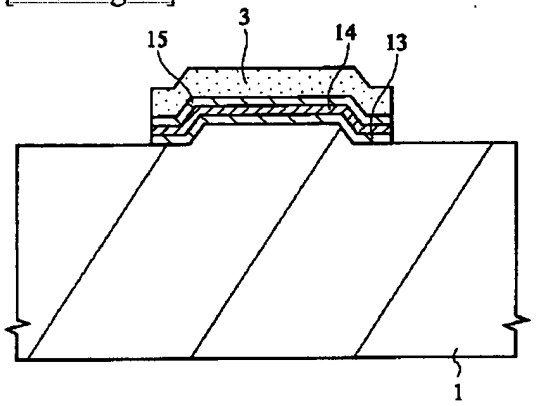
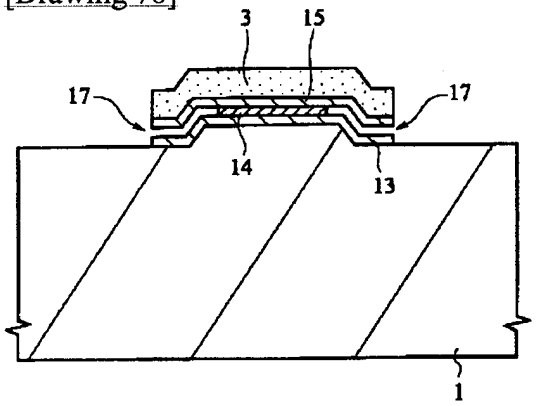


[Drawing 78]



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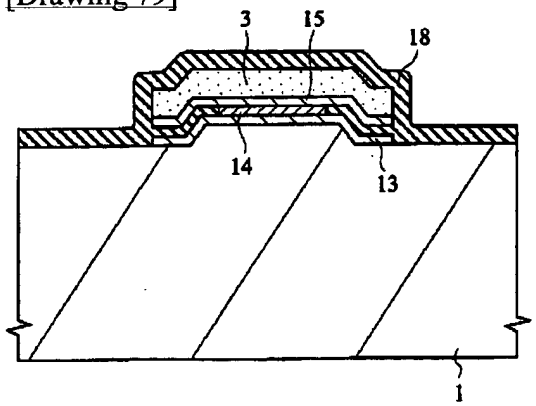

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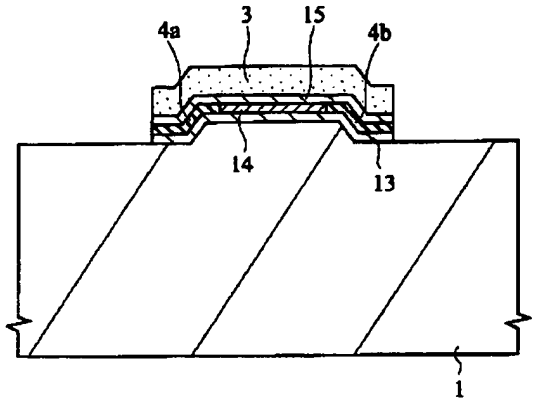

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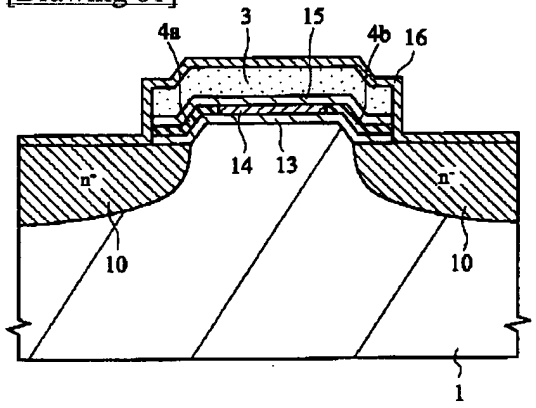

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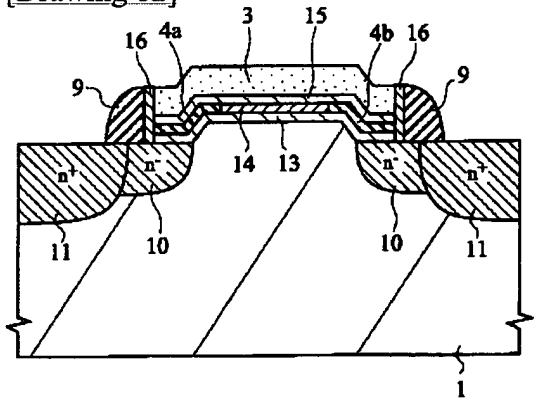

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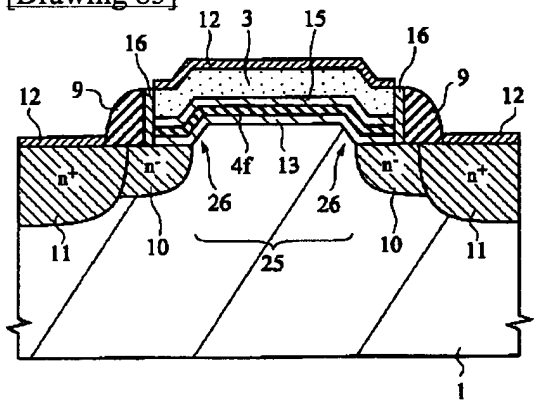

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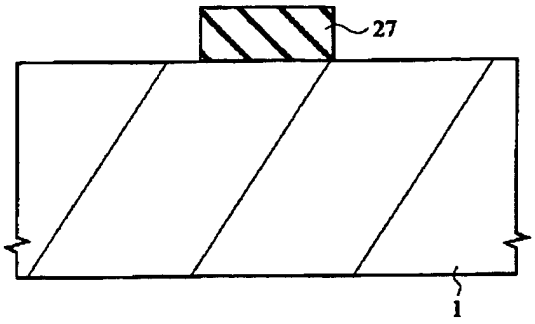

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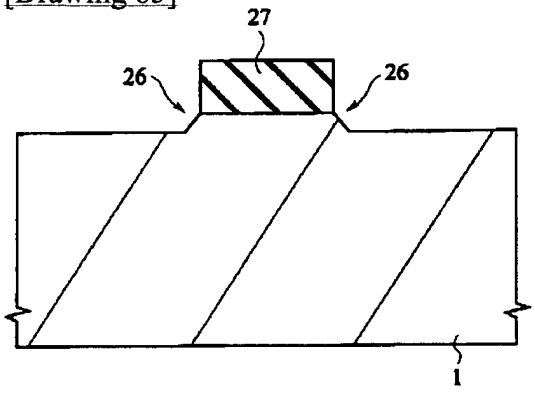

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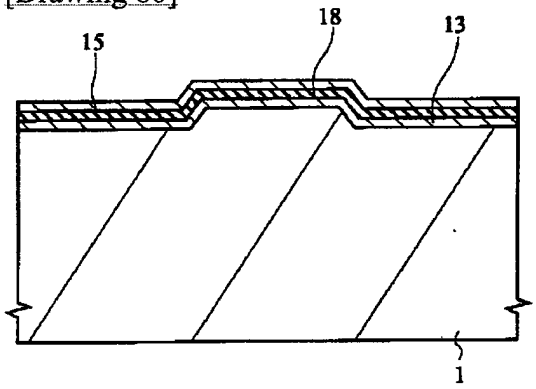

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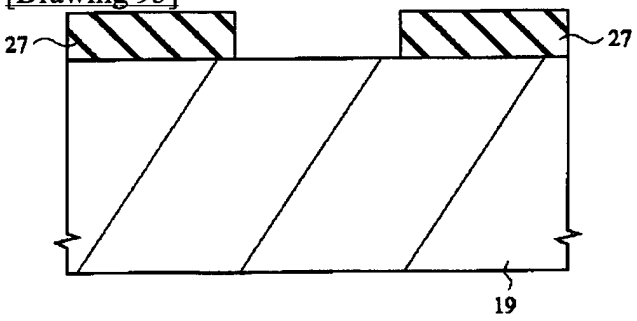

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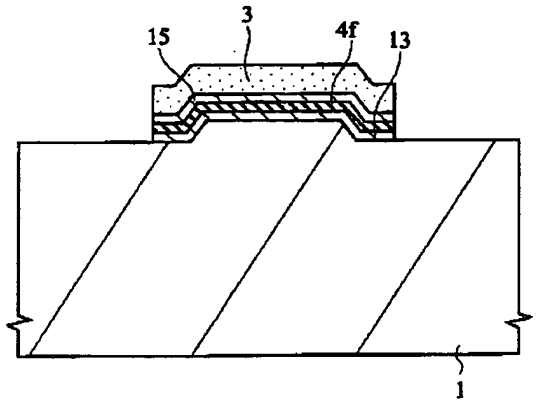

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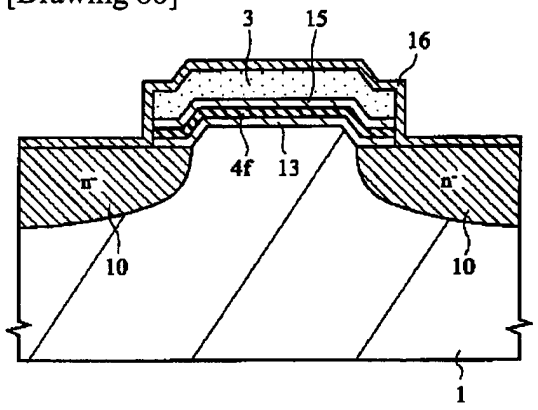

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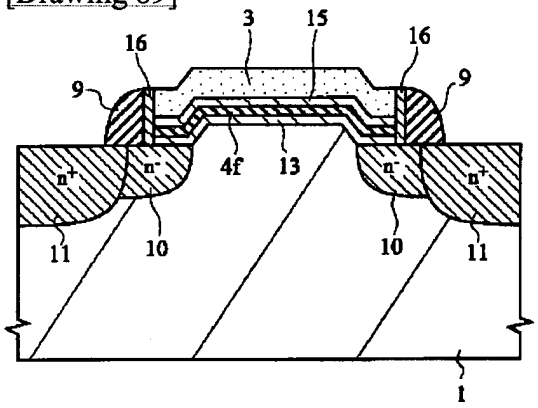

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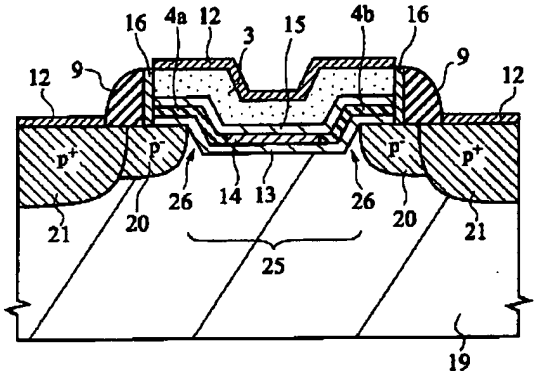

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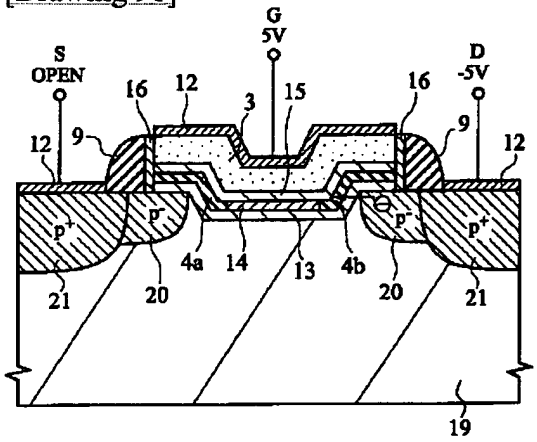

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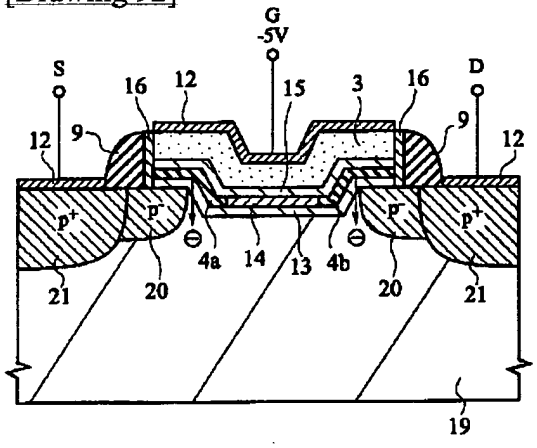

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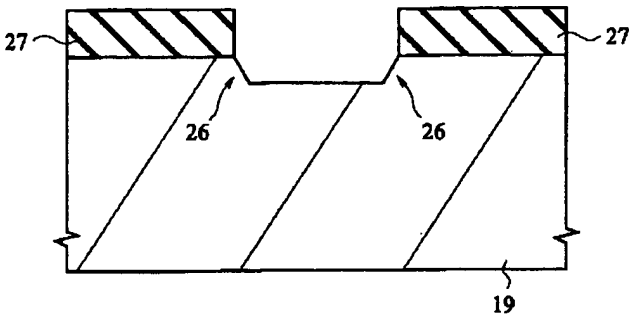

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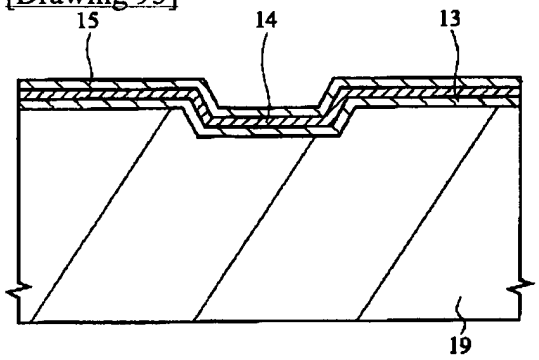

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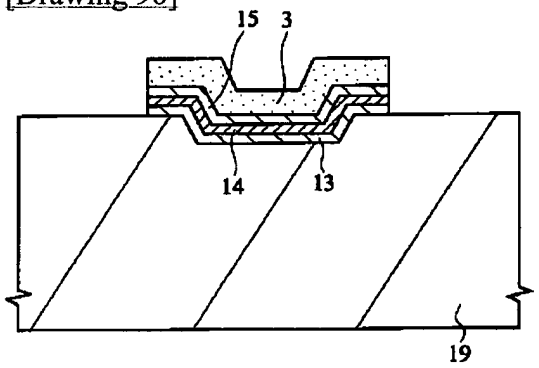

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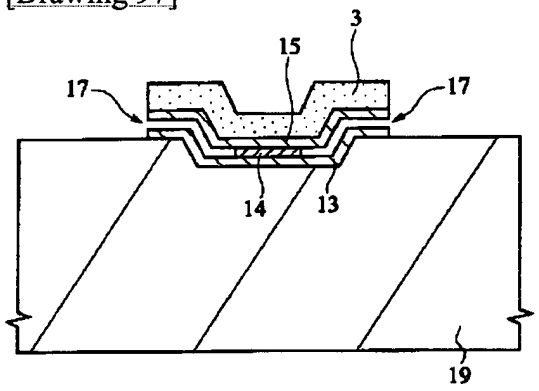

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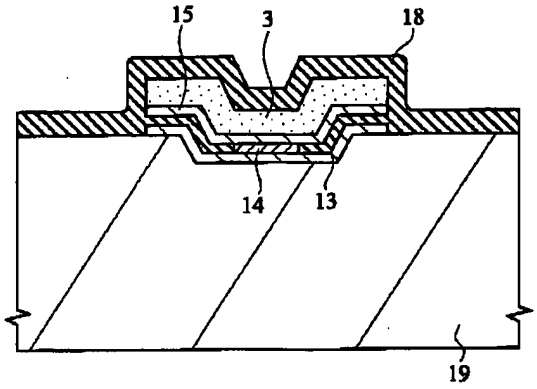

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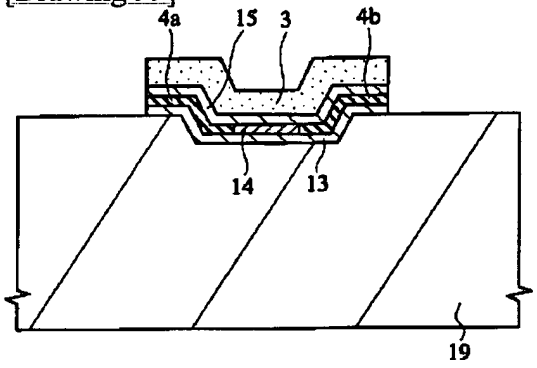

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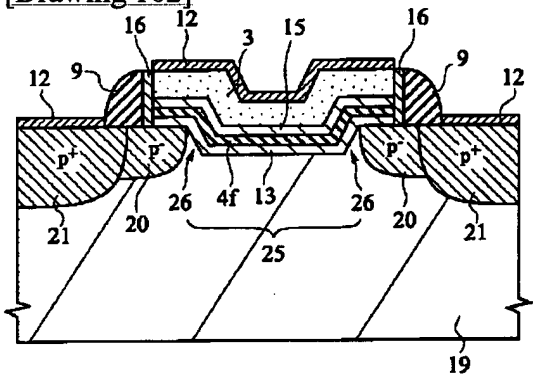

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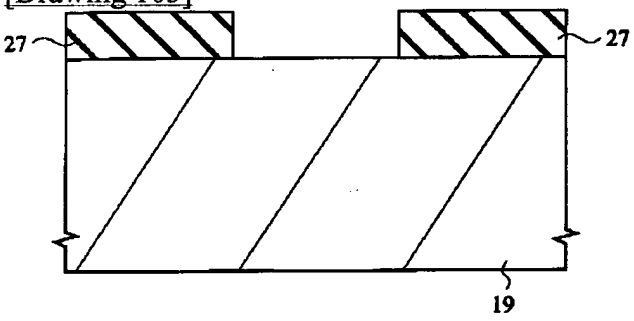

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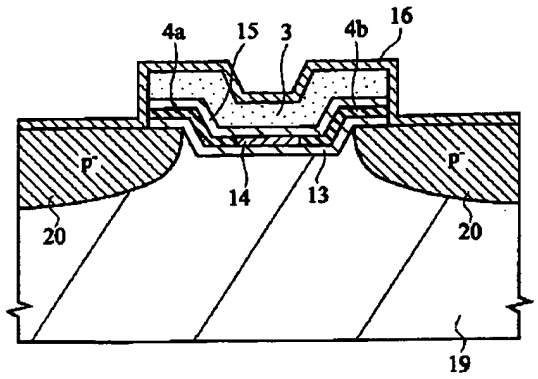

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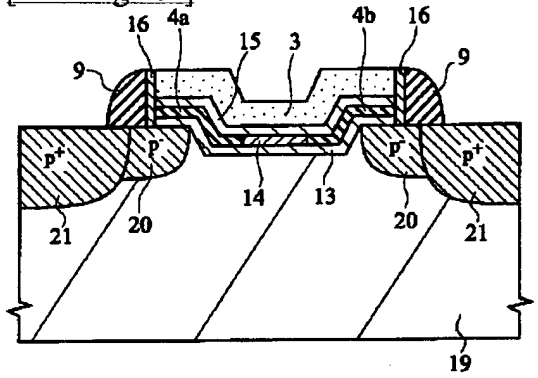

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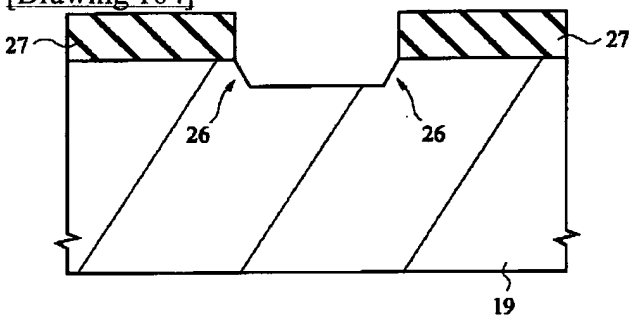

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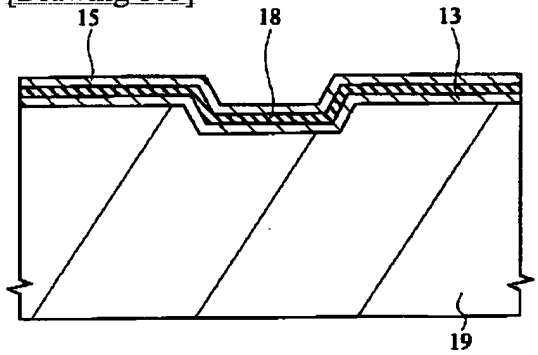

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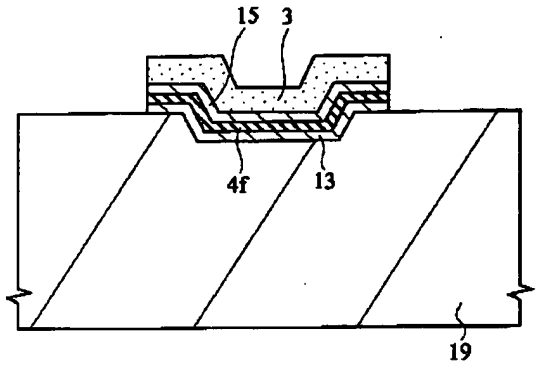

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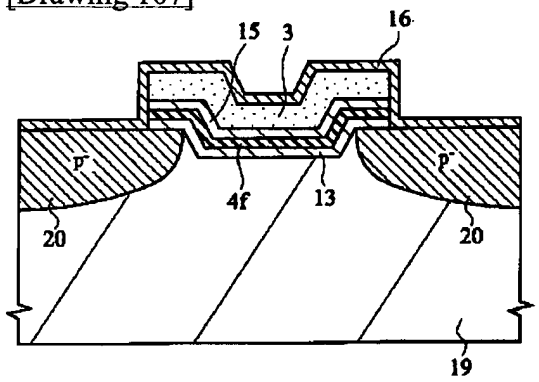

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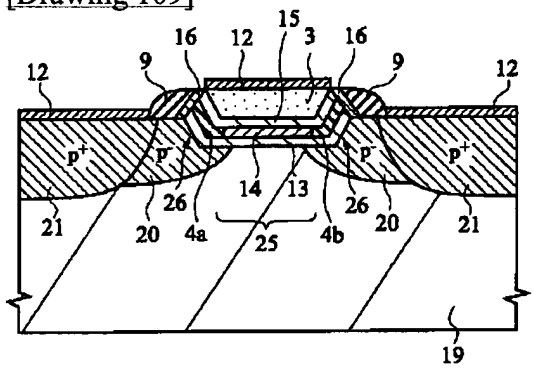

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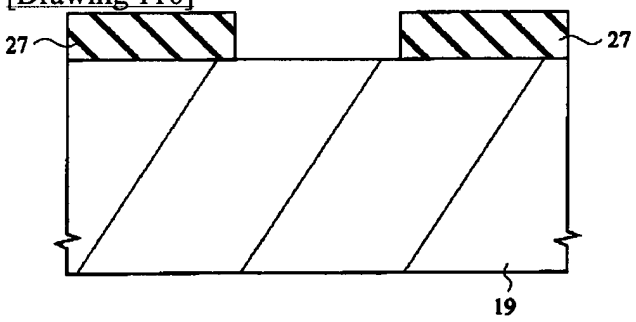

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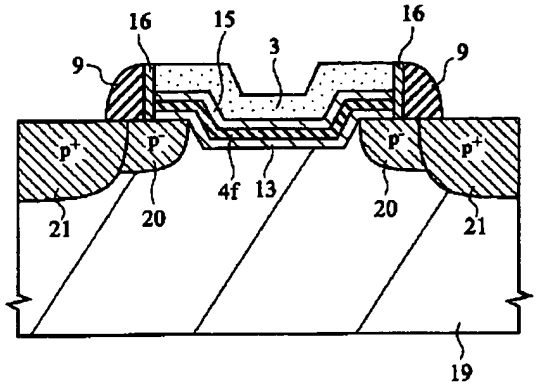

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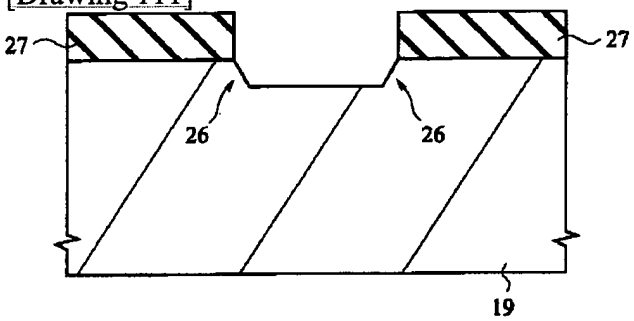

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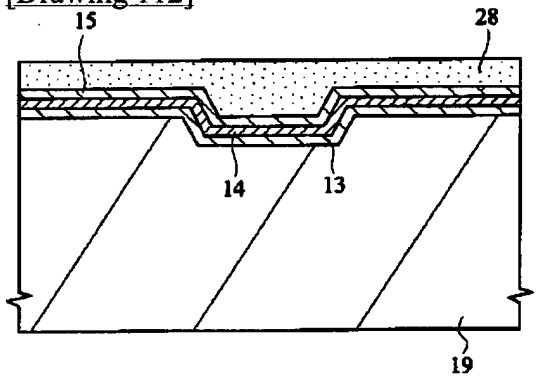

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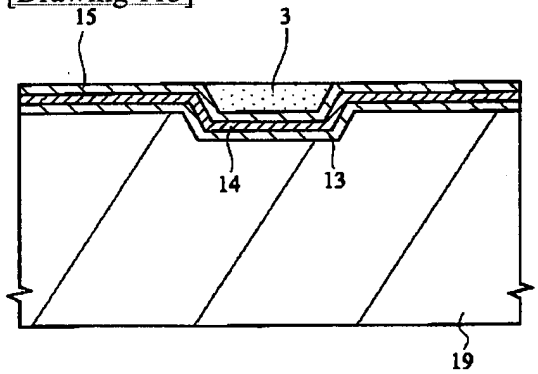

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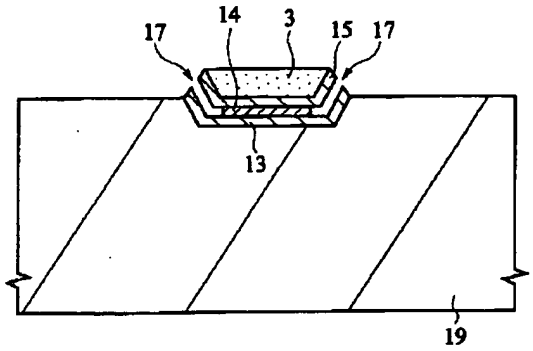

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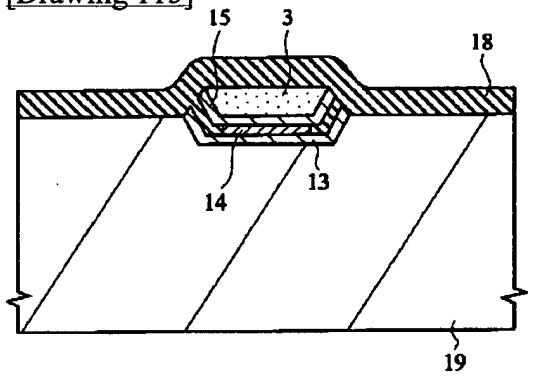

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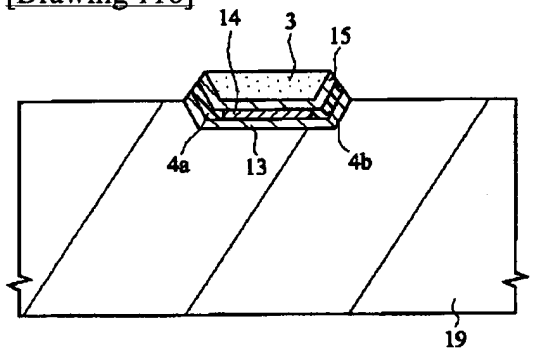

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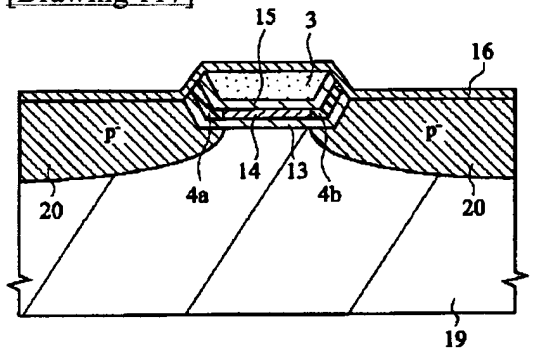

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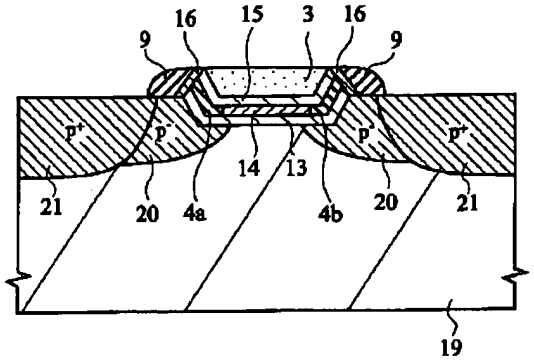

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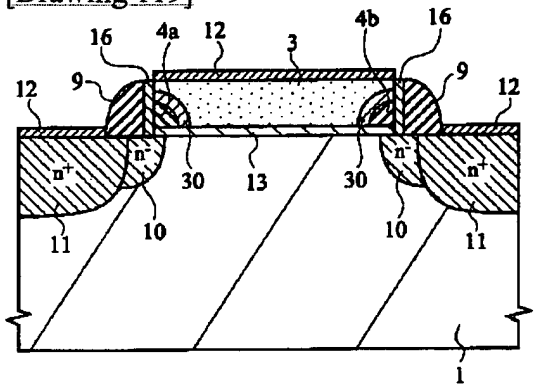

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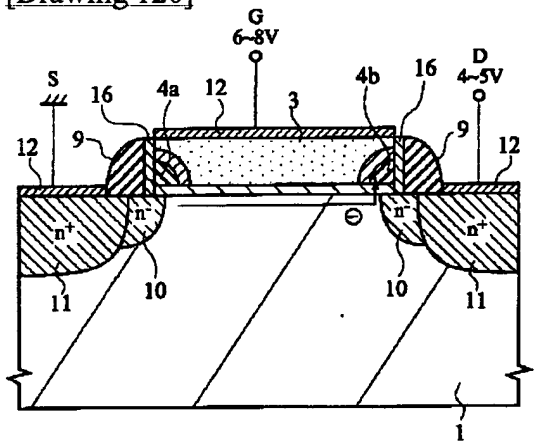

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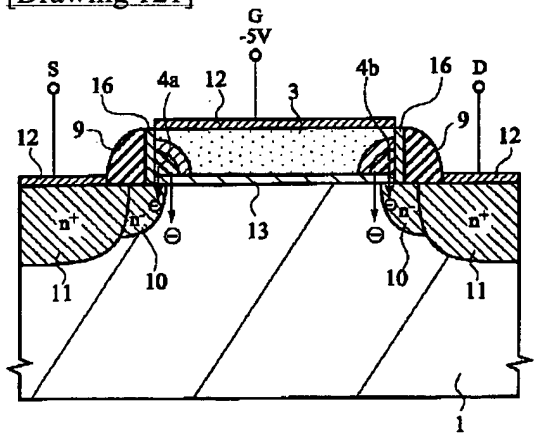

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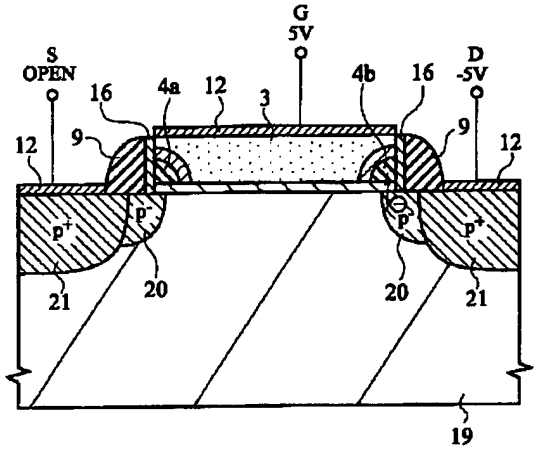

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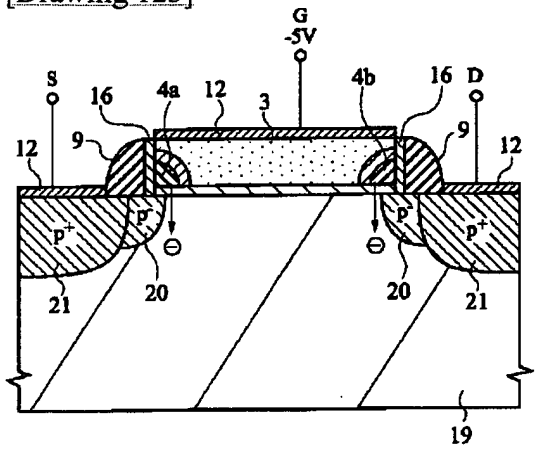

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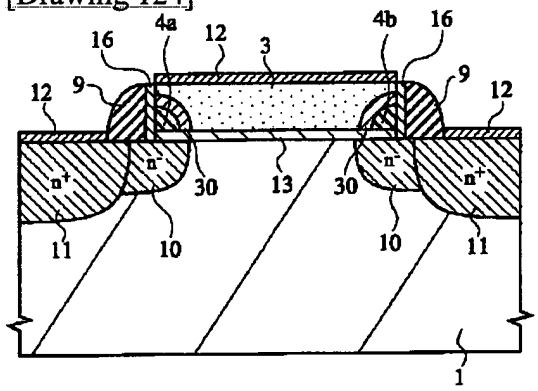

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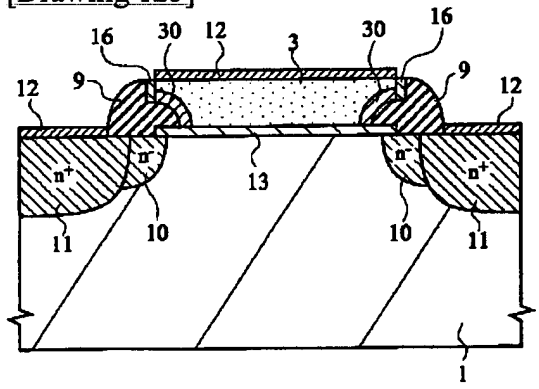

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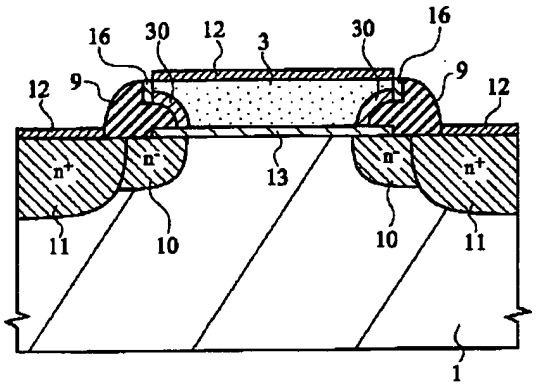

[Translation done.]